TE0720 Test Board

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Overview

Zynq PS Design with Linux Example and PHY status LED on Vivado HW-Manager.

Refer to http://trenz.org/te0720-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2023.2
- PetaLinux
- SD
- ETH (use EEPROM MAC)
- USB
- I2C
- RTC
- VIO PHY LED
- FSBL for EEPROM MAC and CPLD access / petalinux patch

Revision History

Date	Vivado	Project Built	Authors	Description
2024-01-25	2023.2	TE0720-test_board-vivado_2023.2-build_4_20240124111006.zip TE0720-test_board_noprebuilt-vivado_2023.2-build_4_20240124111006.zip	Manuela Strücker	• Device-Tree patch for single core variants
2024-01-22	2023.2	TE0720-test_board-vivado_2023.2-build_4_20240122114822.zip TE0720-test_board_noprebuilt-vivado_2023.2-build_4_20240122114822.zip	Manuela Strücker	• 2023.2 update
2023-07-19	2022.2	TE0720-test_board-vivado_2022.2-build_2_20230719115741.zip TE0720-test_board_noprebuilt-vivado_2022.2-build_2_20230719115741.zip	Waldemar Hanemann	• bugfix -boot up on first power up only. qspi x4 - device tree node entry

2023-05-31	2022.2	TE0720-test_board-vivado_2022.2-build_1_20230531192416.zip TE0720-test_board_noprebuilt-vivado_2022.2-build_1_20230531192416.zip	Waldemar Hanemann	• 2022.2 update
2022-02-02	2021.2	TE0720-test_board-vivado_2021.2-build_11_20220202131818.zip TE0720-test_board_noprebuilt-vivado_2021.2-build_11_20220202131838.zip	Manuela Strücker	• bugfix "os" folder • updated Petalinux config ○ added QSPI Partition for bootscr file
2022-01-25	2021.2	TE0720-test_board-vivado_2021.2-build_10_20220125090947.zip TE0720-test_board_noprebuilt-vivado_2021.2-build_10_20220125090947.zip	Manuela Strücker	• 2021.2 update
2021-12-15	2020.2	TE0720-test_board-vivado_2020.2-build_9_20211215123235.zip TE0720-test_board-vivado_2020.2-build_9_20211215123235_production.zip	Manuela Strücker	• new Assembly variants
2021-11-29	2020.2	TE0720-test_board-vivado_2020.2-build_9_20211129062154.zip TE0720-test_board_noprebuilt-vivado_2020.2-build_9_20211129062716.zip	Manuela Strücker	• new Assembly variants
2021-07-19	2020.2	TE0720-test_board_noprebuilt-vivado_2020.2-build_6_20210719131800.zip TE0720-test_board-vivado_2020.2-build_6_20210719131744.zip	Manuela Strücker	• boot.scr file updated for 256 MB QSPI flash size variants
2021-04-30	2020.2	TE0720-test_board_noprebuilt-vivado_2020.2-build_5_20210430085624.zip TE0720-test_board-vivado_2020.2-build_5_20210430085609.zip	Manuela Strücker	• update board files • update boot. scr file

2021-04-01	2020.2	TE0720-test_board_noprebuilt-vivado_2020.2-build_4_20210401140444.zip TE0720-test_board-vivado_2020.2-build_4_20210401140432.zip	John Hartfiel	• bugfix missing binaries+ boot.scr file (supports now QSPI and SD boot with image.ub on SD)
2021-02-17	2020.2	TE0720-test_board_noprebuilt-vivado_2020.2-build_2_20210217064925.zip TE0720-test_board-vivado_2020.2-build_2_20210217064913.zip	John Hartfiel	• 2020.2 update • add boot.scr file • petalinux fsbl patch (beta-version)
2020-03-25	2019.2	TE0720-test_board_noprebuilt-vivado_2019.2-build_8_20200325075220.zip TE0720-test_board-vivado_2019.2-build_8_20200325075301.zip	John Hartfiel	• script update
2020-01-22	2019.2	TE0720-test_board-vivado_2019.2-build_3_20200122154933.zip TE0720-test_board_noprebuilt-vivado_2019.2-build_3_20200122154951.zip	John Hartfiel	• script update for linux user
2020-01-14	2019.2	TE0720-test_board-vivado_2019.2-build_3_20200114090828.zip TE0720-test_board_noprebuilt-vivado_2019.2-build_3_20200114090837.zip	John Hartfiel	• Vitis script updates (include linux domain and prebuilt linux files for vitis) • prebuilt binary export on selection guide
2019-12-18	2019.2	TE0720-test_board-vivado_2019.2-build_1_20191218151902.zip TE0720-test_board_noprebuilt-vivado_2019.2-build_1_20191218152732.zip	John Hartfiel	• 2019.2 update • Vitis support
2019-03-04	2018.3	TE0720-test_board-vivado_2018.3-build_01_20190304100745.zip TE0720-test_board_noprebuilt-vivado_2018.3-build_01_20190304100755.zip	John Hartfiel	• update for -1 CR version only (256MB DDR3)

2019-02-21	2018.3	TE0720-test_board-vivado_2018.3-build_01_20190221125123.zip TE0720-test_board_noprebuilt-vivado_2018.3-build_01_20190221125133.zip	John Hartfiel	• TE Script update • rework of the FSBLs • some additional Linux features
2018-08-23	2018.2	te0720-test_board-vivado_2018.2-build_03_20180823185142.zip te0720-test_board_noprebuilt-vivado_2018.2-build_03_20180823185158.zip	John Hartfiel	• DDR setup bugfix for l1if only
2018-08-13	2018.2	te0720-test_board-vivado_2018.2-build_02_20180810162024.zip te0720-test_board_noprebuilt-vivado_2018.2-build_02_20180810162040.zip	John Hartfiel	• 2018.2 update • Board Part Files rework
2018-04-26	2017.4	te0720-test_board-vivado_2017.4-build_07_20180426144351.zip te0720-test_board_noprebuilt-vivado_2017.4-build_07_20180426144405.zip	John Hartfiel	• new assembly variant
2018-03-12	2017.4	te0720-test_board_noprebuilt-vivado_2017.4-build_06_20180312152408.zip te0720-test_board-vivado_2017.4-build_06_20180312152419.zip	John Hartfiel	• add assembly variant • script update
2018-01-09	2017.4	te0720-test_board_noprebuilt-vivado_2017.4-build_02_20180109121313.zip te0720-test_board-vivado_2017.4-build_02_20180109121300.zip	John Hartfiel	• no design changes • set EEPROM MAC with FSBL+u-boot • FSBL for QSPI Programming
2017-11-27	2017.2	te0720-test_board_noprebuilt-vivado_2017.2-build_05_20171127153028.zip te0720-test_board-vivado_2017.2-build_05_20171127153006.zip	John Hartfiel	• remove duplicated content

2017-11-20	2017.2	te0720-test_board_noprebuilt-vivado_2017.2-build_05_20171122074701.zip te0720-test_board-vivado_2017.2-build_05_20171122074646.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
QSPI Flash	Programming QSPI fails with Vivado 2021.2	use Vivado 2020.2 or 2019.2 for programming	
TE0720-test_board_noprebuilt-vivado_2020.2-build_2_20210217064925.zip TE0720-test_board-vivado_2020.2-build_2_20210217064913.zip	Linux binaries are missing boot.scr are only prepared for SD Boot	create and modify by yourself or use 2019.2 design	solved with 2020-04-01 update
Variant with 256MB DDR only(TE0720-03-1CR)	wrong netboot offset	recreate u-boot on petalinux with reduced netboot offset only	solved with 2019-03-04 update

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation
PetaLinux	2023.2	needed

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0720-03-1CF*	1cf_1gb	REV03|REV02	1GB	32MB	4GB	NA	NA

TE0720-03-14S-1C	14s_1gb	REV03|REV02	1GB	32MB	4GB	NA	NA
TE0720-03-1CFA	1cf_1gb	REV03|REV02	1GB	32MB	8GB	NA	NA
TE0720-03-1CR	1cr_256mb	REV03|REV02	256MB	32MB	NA	NA	NA
TE0720-03-1QF	1qf_1gb	REV03|REV02	1GB	32MB	4GB	NA	NA
TE0720-03-1QFA	1qf_1gb	REV03|REV02	1GB	32MB	4GB	NA	NA
TE0720-03-1QFL	1qf_1gb	REV03|REV02	1GB	32MB	4GB	2.5 mm connectors	low profile
TE0720-03-1QFY	1qf_1gb	REV03	1GB	32MB	4GB	NA	no RTC
TE0720-03-2IF	2if_1gb	REV03|REV02	1GB	32MB	4GB	NA	NA
TE0720-03-2IFA	2if_1gb	REV03|REV02	1GB	32MB	4GB	NA	NA
TE0720-03-2IFC3	2if_1gb	REV03|REV02	1GB	32MB	4GB	2.5 mm connectors	low profile
TE0720-03-2IFC8	2if_1gb	REV03|REV02	1GB	32MB	32GB	NA	NA
TE0720-03-31C33FA	14s_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-31C33MA	14s_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61C33FA	1cf_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61C33MA	1cf_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61C33MAS	1cf_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61C33MAY	1cf_1gb	REV03	1GB	32MB	8GB	NA	no RTC
TE0720-03-61C530A	1cr_256mb	REV03	256MB	32MB	NA	NA	NA
TE0720-03-61Q33FA	1qf_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61Q33FAE	1qf_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61Q33FL	1qf_1gb	REV03	1GB	32MB	8GB	2.5 mm connectors	low profile
TE0720-03-61Q33MA	1qf_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-61Q33MAY	1qf_1gb	REV03	1GB	32MB	8GB	NA	no RTC
TE0720-03-61Q33ML	1qf_1gb	REV03	1GB	32MB	8GB	2.5 mm connectors	low profile
TE0720-03-61Q42GA	1qf_256mb	REV03	256MB	32MB	32GB	NA	NA
TE0720-03-61Q42GAY	1qf_256mb	REV03	256MB	32MB	32GB	NA	no RTC
TE0720-03-61Q43FA	1qf_256mb	REV03	256MB	32MB	8GB	NA	NA
TE0720-03-61Q43GA	1qf_256mb	REV03	256MB	32MB	32GB	NA	NA
TE0720-03-61Q43MA	1qf_256mb	REV03	256MB	32MB	8GB	NA	automotive Zynq and DDR

TE0720-03-61Q86KL	1qf_1gb	REV03	1GB	32MB	8GB	NA	Automotive DDR and QSPI
TE0720-03-62I12GA	2if_1gb	REV03	1GB	32MB	32GB	NA	NA
TE0720-03-62I320M	2if_1gb	REV03	1GB	32MB	NA	NA	CAO: no Eth, USB, RTC, VBAT, CryptoKey
TE0720-03-62I33-V1	2if_1gb	REV03	1GB	32MB	NA	NA	NA
TE0720-03-62I330M	2if_1gb	REV03	1GB	32MB	NA	NA	CAO: no Eth, USB, RTC, VBAT, CryptoKey
TE0720-03-62I33FA	2if_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-62I33FL	2if_1gb	REV03	1GB	32MB	8GB	2.5 mm connectors	low profile
TE0720-03-62I33GA	2if_1gb	REV03	1GB	32MB	32GB	NA	NA
TE0720-03-62I33MA	2if_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-62I33MAN	2if_1gb	REV03	1GB	32MB	8GB	NA	NA
TE0720-03-62I33MAY	2if_1gb	REV03	1GB	32MB	8GB	NA	no RTC
TE0720-03-62I33ML	2if_1gb	REV03	1GB	32MB	8GB	2.5 mm connectors	low profile
TE0720-03-62I33NA	2if_1gb	REV03	1GB	32MB	32GB	NA	NA
TE0720-03-64I63FA	l1if_512mb	REV03	512MB	32MB	8GB	NA	LP DDR3
TE0720-03-L1IF	l1if_512mb	REV03|REV02	512MB	32MB	4GB	NA	LP DDR3
TE0720-03-S006C1	1qf_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S007C1	1qf_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S008C1	1qf_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S009C1	1qf_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S010	1qf_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S011	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO: no ETH
TE0720-03-S012	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S013	1cf_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S014	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S016	1cr_256mb	REV03	256MB	32MB	NA	NA	CAO: no RTC
TE0720-03-S017	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO: no RTC
TE0720-03-S020	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-03-S032	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO

TE0720-04-31C33MA	14s_1gb	REV04	1GB	32MB	8GB	NA	NA
TE0720-04-61C33MA	1cf_1gb	REV04	1GB	32MB	8GB	NA	NA
TE0720-04-61C530A	1cr_256mb	REV04	256MB	32MB	NA	NA	NA
TE0720-04-61Q33MA	1qf_1gb	REV04	1GB	32MB	8GB	NA	NA
TE0720-04-61Q33ML	1qf_1gb	REV04	1GB	32MB	8GB	2.5 mm connectors	low profile
TE0720-04-61Q43MA	1qf_256mb	REV04	256MB	32MB	8GB	NA	automotive Zynq and DDR
TE0720-04-61Q86PL	1qf_1gb	REV04	1GB	32MB	8GB	NA	Automotive DDR and QSPI
TE0720-04-62I33MA	2if_1gb	REV04	1GB	32MB	8GB	NA	NA
TE0720-04-62I33MAN	2if_1gb	REV04	1GB	32MB	8GB	NA	NA
TE0720-04-62I33ML	2if_1gb	REV04	1GB	32MB	8GB	2.5 mm connectors	low profile
TE0720-04-62I33NA	2if_1gb	REV04	1GB	32MB	32GB	NA	NA
TE0720-04-64I63MA	l1if_512mb	REV04	512MB	32MB	8GB	NA	LP DDR3
TE0720-04-S001C1	1qf_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S007C1	1qf_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S016	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S019	1cf_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S022	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S023	2if_1gb	REV03	1GB	32MB	8GB	NA	CAO
TE0720-04-S025	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S026	2ef_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S027	2if_1gb	REV04	1GB	32MB	8GB	2.5 mm connectors	CAO and low profile
TE0720-04-S028	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S029	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S030	2if_1gb	REV04	1GB	32MB	32GB	NA	CAO
TE0720-04-S031	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S032	1qf_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S033	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S034	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S035	1cf_1gb	REV04	1GB	32MB	8GB	NA	CAO

TE0720-04-S036	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO
TE0720-04-S037	2if_1gb	REV04	1GB	32MB	8GB	NA	CAO

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TE0703*	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers • Used as reference carrier.
TE0705	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TE0706	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers
TEBA0841	• See restrictions on usage with 7 Series Carriers: 4 x 5 SoM Carriers • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Additional Hardware

Content

For general structure and usage of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File

OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0720 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-----------------------TE Reference
Design-------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
    - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
    - use TE Template from "<project folder>\os\petalinux"
    - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
    - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Generate Programming Files with Vitis (recommended)
    a. Copy PetaLinux build image files to prebuilt folder
        - copy **u-boot.elf**, **system.dtb**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

> "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

b. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE Scripts on Vivado TCL)
```

> TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

8. Generate Programming Files with Petalinux (alternative), see PetaLinux KICKstart

Launch

Programming

> Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select create and open delivery binary folder

> Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp u-boot
TE::pr_program_flash -swapp hello_te0720 (optional)
```


To program with Vitis/Vivado GUI, use special FSBL (fsbl_flash) on setup

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
    - Depends on Carrier, see carrier TRM.

SD-Boot mode

1. Copy **image.ub**, **boot.src** and **Boot.bin** on **SD**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
    - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

Note: See TRM of the Carrier, which is used.

Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
The boot options described above describe the common boot processes for this hardware; other boot options are possible.
For more information see Distro Boot with Boot.scr

4. Power On PCB

    1. Zynq Boot ROM loads FSBL from SD/QSPI into OCM,

    2. FSBL init PS, programs PL using the bitstream and loads U-boot from SD into DDR,

    3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)
    - Speed: 115200
    - select COM Port

    > Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

    (can be skipped with config auto login in petalinux)

    ```
    # password disabled
    petalinux login: root
    Password: root
    ```

    > Note: Wait until Linux boot finished

3. You can use Linux shell now.

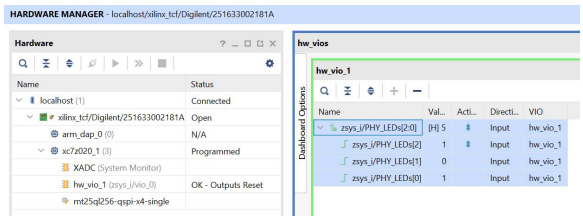
    ```
    i2cdetect -y -r 0        (check I2C 0 Bus)
    i2cdetect -y -r 1        (check I2C 1 Bus)
    dmesg | grep rtc        (RTC check)
    udhcpc                                (ETH0 check)
    lsusb                                (USB check)
    ```

4. Option Features
    - Webserver to get access to Zynq
        - insert IP on web browser to start web interface
    - init.sh scripts
        - add init.sh script on SD, content will be load automatically on startup (template is included in "<project folder>\misc\SD")

Vivado HW Manager

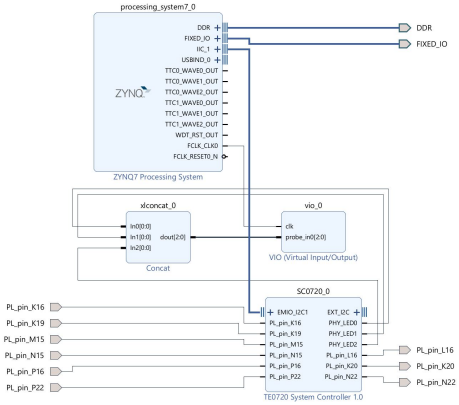
Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Monitoring: PHY LED



System Design - Vivado

Block Design



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	---
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
I2C1	EMIO
UART0	MIO
UART1	MIO
GPIO	MIO
SWDT	EMIO
TTC0..1	EMIO
ETH0	MIO
USB0	MIO

PS Interfaces

Constraints

Basic module constraints

_i_bitgen_common.xdc

```
#
# Common BITGEN related settings for TE0720 SoM
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
```

_i_common.xdc

```
#
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLUP [current_design]
```

Design specific constraints

_i_TE0720-SC.xdc

```
#
# Constraints for System controller support logic
#
set_property PACKAGE_PIN K16 [get_ports PL_pin_K16]
set_property PACKAGE_PIN K19 [get_ports PL_pin_K19]
set_property PACKAGE_PIN K20 [get_ports PL_pin_K20]
set_property PACKAGE_PIN L16 [get_ports PL_pin_L16]
set_property PACKAGE_PIN M15 [get_ports PL_pin_M15]
set_property PACKAGE_PIN N15 [get_ports PL_pin_N15]
set_property PACKAGE_PIN N22 [get_ports PL_pin_N22]
set_property PACKAGE_PIN P16 [get_ports PL_pin_P16]
set_property PACKAGE_PIN P22 [get_ports PL_pin_P22]

#
# If Bank 34 is not 3.3V Powered need change the IOSTANDARD
#
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_P16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N22]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_N15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_M15]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_L16]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K20]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K19]
set_property IOSTANDARD LVCMOS33 [get_ports PL_pin_K16]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
  - READ MAC from EEPROM and make Address accessible by UBOOT (need copy defines on uboot platform-top.h)
  - CPLD access
  - Read CPLD Firmware and SoC Type
  - Configure Marvell PHY
  - USB PHY Reset
  - Configure LED usage

hello_te0720

Hello TE0720 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_SERIAL_PS7_UART_0_SELECT=y
- CONFIG_SUBSYSTEM_SERIAL_IP_NAME="ps7_uart_0"
- CONFIG_SUBSYSTEM_FSBL_SERIAL_PS7_UART_0_SELECT=y
- # CONFIG_SUBSYSTEM_FSBL_SERIAL_PS7_UART_1_SELECT is not set
- CONFIG_SUBSYSTEM_SERIAL_FSBL_IP_NAME="ps7_uart_0"
- CONFIG_SUBSYSTEM_MEMORY_PS7_DDR_0_BANKLESS_U__BOOT_TEXTBASE_OFFSET=0x100000
- add new flash partition for bootscr and sizing
  - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART0_SIZE=0x0100000
  - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART1_SIZE=0x1400000
  - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART2_SIZE=0x0020000
  - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART3_NAME="bootscr"
  - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART3_SIZE=0x40000
- Identification

    - CONFIG_SUBSYSTEM_HOSTNAME="Trenz"
    - CONFIG_SUBSYSTEM_PRODUCT="TE0720"

Note: for variants with 256MB DDR only, change NET Boot Address to 0x8000000 on **boot.src** file

U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
    - CONFIG_ENV_OVERWRITE=y
    - CONFIG_PREBOOT="echo U-BOOT for petalinux;echo Importing env from FSBL shared area at 0xFFFFFC00;if test *0xFFFFFC00 == 0xCAFEBABE;then echo Found valid magic; env import -t 0xFFFFFC04; fi;setenv preboot; echo;"
- Boot Modes:
    - CONFIG_QSPI_BOOT=y
    - CONFIG_SD_BOOT=y
    - CONFIG_BOOT_SCRIPT_OFFSET=0x1520000
      (Calculate the start address of partition 3 "bootscr" in the QSPI flash. To do this, add the sizes of partitions 0, 1 and 2 together)
- Identification
    - CONFIG_IDENT_STRING=" TE0720"

Device Tree

Device Tree (system-user.dtsi in device-tree and uboot-device-tree)

```
/include/ "system-conf.dtsi"
/ {
};


/* bugfix */
/* Uncomment on usage with single core variant only */
/*
&amba {
    ptm@f889d000 {
        cpu = <&cpu0>;
    };
};
*/

/* default */

/*------------------ QSPI PHY --------------------*/
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;

        spi-rx-bus-width = <4>;
```

```
        spi-tx-bus-width = <4>;
        spi-max-frequency = <90000000>;
    };
};


/*-------------------- ETH PHY ----------------*/
&gem0 {
    phy-handle = <&phy0>;
    mdio {
        #address-cells = <1>;
        #size-cells = <0>;

        phy0: phy@0 {
            compatible = "marvell,88e1510";
            device_type = "ethernet-phy";
            reg = <0>;
        };
    };
};


/*-------------------- USB PHY ----------------*/
/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        //compatible = "usb-nop-xceiv";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/* I2C need I2C1 connected to te0720 system controller ip */
&i2c1 {

    iexp@20 {       // GPIO in CPLD
        #gpio-cells = <2>;
        compatible = "ti,pcf8574";
        reg = <0x20>;
        gpio-controller;
    };

    iexp@21 {       // GPIO in CPLD
        #gpio-cells = <2>;
        compatible = "ti,pcf8574";
        reg = <0x21>;
        gpio-controller;
    };

    /* Commend out if no RTC is fitted */
    rtc@6F {        // Real Time Clock
        compatible = "isl12022";
        reg = <0x6F>;
```

```
    };
};
```

Device Tree patch (for single core variant)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\device-tree\files\"

Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_RTC_DRV_ISL12022=y

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
  - CONFIG_busybox-httpd=y
- For additional test tools only:
  - CONFIG_i2c-tools=y
  - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
  - CONFIG_util-linux-umount=y
  - CONFIG_util-linux-mount=y
- For usage of phytool:
  - CONFIG_ethtool=y
- For auto login:
  - CONFIG_auto-login=y

Add in "<project folder>\os\petalinux\project-spec\meta-user\conf\petalinuxbsp.conf"

```
IMAGE_INSTALL:append += "\
phytool \
"
```

FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"

Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

startup

Script App to load init.sh from SD Card if available.

webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission.	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission.	• Device-Tree patch for single core variants

Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class

Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class

Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class

com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	
2024-01-22	v.58	Manuela Strücker	• 2023.2 release
2023-07-19	v.57	Waldemar Hanemann	• bugfix -boot up on first power up only. qspi x4 - device tree node entry
2023-07-19	v.56	Waldemar Hanemann	• 2022.2 release
2022-05-09	v.52	Thomas Dück	• bugfix os folder • bugfix table of content

2022-01-25	v.50	Manuela Strücker	• 2021.2 release
2021-12-16	v.49	Manuela Strücker	• new assembly variants
2021-11-29	v.46	John Hartfiel	• new assembly variants
2021-07-19	v.45	Manuela Strücker	• boot.scr file updated for 256 MB QSPI flash size variants
2021-05-25	v.44	Manuela Strücker	• update board files • update boot.scr file
2021-04-01	v.42	John Hartfiel	• Design update
2021-02-26	v.41	John Hartfiel	• add issue notes
2021-02-17	v.40	John Hartfiel	• 2020.2 release
2020-03-25	v.39	John Hartfiel	• script update
2020-01-22	v.38	John Hartfiel	• script update for linux user
2020-01-14	v.37	John Hartfiel	• Vitis script updates (include linux domain and prebuilt linux files for vitis) • prebuilt binary export on selection guide
2019-12-19	v.36	John Hartfiel	• 2019.2 release
2019-12-03	v.34	John Hartfiel	• bugfix document link
2019-10-28	v.33	John Hartfiel	• removed remove instructions that are no longer used
2019-05-07	v.31	John Hartfiel	• Some FSBL notes • wrong link

2019-03-06	v.28	John Hartfiel	• Fixed prebuilt issue for TE0720-03-1CR
2019-03-01	v.27	John Hartfiel	• Known issue for TE0720-03-1CR linux design
2019-02-21	v.26	John Hartfiel	• 2018.3 release finished (include design reworks)
2018-08-30	v.25	John Hartfiel	• update documentation PS configuration
2018-08-23	v.24	John Hartfiel	• update l1if board parts
2018-08-13	v.23	John Hartfiel	• 2018.4 release
2018-04-26	v.22	John Hartfiel	• add assembly variant
2018-02-20	v.20	John Hartfiel	• small documentation update
2018-01-09	v.16	John Hartfiel	• Release 2017.4 • Documentation update
2017-11-27	v.14	John Hartfiel	• Typo correction • Design Files update
2017-11-22	v.12	John Hartfiel	• Update HW list
2017-11-22	v.11	John Hartfiel	• Release 2017.2
2017-11-20	v.1	**Error renderi ng macro 'page-info'**	• Initial release

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between

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atlassian . confluence. pages. Page] due to overlapping prototypes between : [interface com. atlassian . confluence.user. ConfluenceUser, class java. lang. String, class com. atlassian . confluence.core. ContentEntityObject] [interface com. atlassian .user. User,

		class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

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Error rendering macro 'page-info'

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