TEI0001 Test Board

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Overview

Nios V/m design example with SDRAM controller (AXI4), flash memory, 3-axis Accelerometer and different LED sequences.

Refer to http://trm.tebeans.com/tei0001/ for the current online version of this manual and other available documentation.

Key Features

- Quartus Prime Lite 22.1std
- Nios V/m
- UART
- Flash memory
- SDRAM controller (AXI4)
  - Source code: https://github.com/ultraembedded/core_sdram_axi4
- 3-axis Accelerometer
- User LEDs
- User buttons

Revision History

Date	Quartus	Project Built	Authors	Description
2024-02-07	22.1 Lite	TEI0001-test_board_noprebuilt-quartus_22.1std.2-20240207162519.zip TEI0001-test_board-quartus_22.1std.2-20240207162631.zip	Thomas Dück	• update to Quartus Prime Lite 22.1 • new board variants • change to Nios V/m • TE scripts update
2022-04-21	21.1 Lite	TEI0001-test_board_noprebuilt-quartus_21.1.0-20220421150137.zip TEI0001-test_board-quartus_21.1.0-20220421150228.zip	Thomas Dück	• update to Quartus Prime Lite 21.1
2021-07-09	20.1 Lite	TEI0001-test_board_noprebuilt-quartus_20.1.1-20210709113727.zip TEI0001-test_board-quartus_20.1.1-20210709113644.zip	Thomas Dück	• update to Quartus Prime Lite 20.1 • TE scripts update

2020-10-19	19.1 Lite	TEI0001-test_board_noprebuilt-quartus_19.1.0-20201019101714.zip TEI0001-test_board-quartus_19.1.0-20201019101651.zip	Thomas Dück	• bugfixes
2020-07-07	19.1 Lite	TEI0001-test_board_noprebuilt-quartus_19.1.0-20200707153033.zip TEI0001-test_board-quartus_19.1.0-20200707153205.zip	Thomas Dück	• bugfixes • script update
2020-05-12	19.1 Lite	TEI0001-test_board_noprebuilt-quartus_19.1.0-20200512095852.zip TEI0001-test_board-quartus_19.1.0-20200512100037.zip	Thomas Dück	• 19.1 update
2019-11-11	18.1	TEI0001-test_board_noprebuilt-quartus_18.1-20191111104201.zip TEI0001-test_board-quartus_18.1-20191111104348.zip	Thomas Dück	• add bash files for Linux OS
2019-10-28	18.1	TEI0001-test_board_noprebuilt-quartus_18.1-20191028120819.zip TEI0001-test_board-quartus_18.1-20191028120521.zip	Thomas Dück	• create project with TE scripts • new assembly variants
2019-04-02	18.1	TEI0001-03-08-C8-test_board-quartus_18.1-20190402.zip	Thomas Dück	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note

Quartus Prime Lite	22.1std	Nios V license is needed. For more information see: Intel Nios V Processors
RiscFree IDE for Intel FPGAs	22.1std	needed

Software

Hardware

Complete List is available on <project folder>/board_files/*_devices.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	Flash memory	Others	Notes
TEI0001-02-08-C8*	DBC83	REV02	8Mbyte	8Mbyte	--	--
TEI0001-02-16-C8	FBC83	REV02	8Mbyte	8Mbyte	--	--
TEI0001-03-08-C8	DBC83	REV03	8MByte	8Mbyte	--	--
TEI0001-03-16-C8	FBC83	REV03	8MByte	8Mbyte	--	--
TEI0001-03-16-C8A	FBC84	REV03	32MByte	8Mbyte	--	--
TEI0001-03-DBC83A	DBC83	REV03	8Mbyte	8Mbyte	--	--
TEI0001-03-FBC83A	FBC83	REV03	8Mbyte	8Mbyte	--	--
TEI0001-03-FBC84A	FBC84	REV03	32MByte	8Mbyte	--	--
TEI0001-04-DBC83A	DBC83	REV04	8Mbyte	8Mbyte	--	--
TEI0001-04-FBC83A	FBC83	REV04	8Mbyte	8Mbyte	--	--
TEI0001-04-FBC84A	FBC84	REV04	32MByte	8Mbyte	--	--

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
---	

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
Micro USB cable for JTAG/UART	--

*used as reference

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - Intel devices

Design Sources

Type	Location	Notes
Quartus	<project folder>/source_files /quartus	Quartus project will be generated by TE Scripts
Software	<project folder>/source_files /software	Additional software will be generated by TE Scripts

Design sources

Prebuilt

File	File-Extension	Description
SOPC Information File	*.sopcinfo	File with description of the *. qsys file to create software for the target hardware
Programmer Object File	*.pof	FPGA configuration file
Diverse Reports	---	Report files in different formats
Software Application File	*.elf	Software application for NIOS II processor system
BIN-File	*.bin	Image of the software application for flash memory

Prebuilt files (only on ZIP with prebuilt content)

Download

Reference Design is only usable with the specified Quartus version. Do never use different versions of Quartus software for the same project.

Reference Design is available on:

- TEI0001 "Test Board" Reference Design

Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Quartus Design Flow.

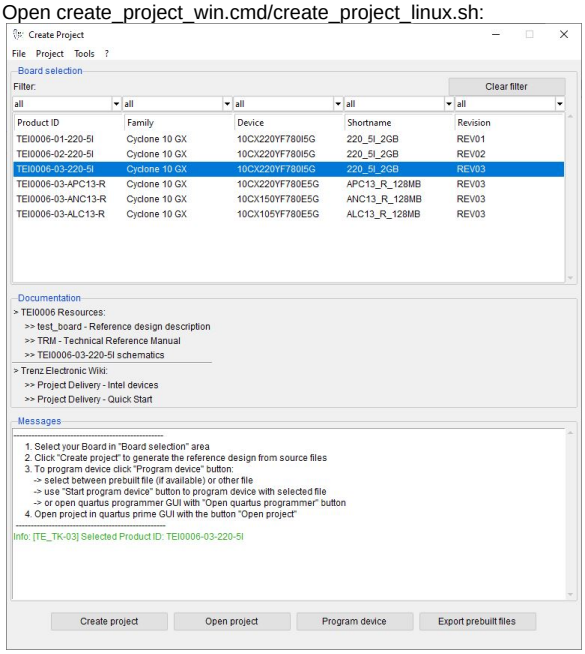
See also:

- Project Delivery - Intel devices

The Trenz Electronic FPGA Reference Designs are TCL-script based projects. To create a project, open a project or program a device execute "create_project_win.cmd" on Windows OS and "create_project_linux.sh" on Linux OS.

TE Scripts are only needed to generate the quartus project, all other additional steps are optional and can also executed by Intel Quartus/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery - Intel devices Currently limitations of functionality

1. Open create_project_win.cmd/create_project_linux.sh:



2. Select Board in "Board selection"
3. Click on "Create project" button to create project
    a. (optional for manual changes) Select correct quartus installation path in *"<project folder>/settings/design_basic_settings.tcl"*

Launch

Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Get prebuilt boot binaries

> ⚠ Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

1. Run create_project_win.cmd/create_project_linux.sh
2. Select Module in 'Board selection'
3. Click on 'Export prebuilt files' button
    a. Folder <*project folder*>/_binaries_<*Article Name*> with subfolder *programming_files* will be generated and opened

MAX10 and flash memory

1. Connect the Module to USB-Port
2. Open create_project_win.cmd/create_project_linux.sh
3. Select correct board in "Board selection"
4. Click on "Program device" button
    a. if prebuilt files are available: select "Program prebuilt file"
        i. Note: With this selection, the MAX10 is programmed with the pof file and the flash memory is also programmed with the bin file
    b. using own generated programming file: select "Program other file" and click on "Browse ..." to open own generated programming file
    c. (optional): click on "Open programmer GUI" to program device with Quartus programmer GUI
5. Click on "Start program device" button

Flash memory only

1. Connect the Module to USB-Port
2. Open create_project_win.cmd/create_project_linux.sh
3. Select correct board in "Board selection"
4. Click on "Program device" button
    a. select "Program other file" and click on "Browse ..." to open the bin file
5. Click on "Start program device" button

Usage

1. Prepare Hardware like described on section Programming
2. Connect UART USB (most cases same as JTAG)

UART

1. Open Serial Console (e.g. PuTTY)
    a. select COM Port

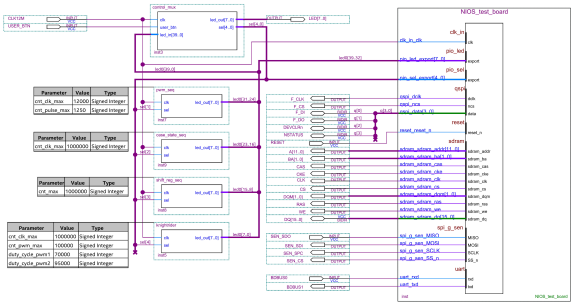
    > ⓘ Win OS: see device manager
    >
    > Linux OS: see dmesg | grep tty (UART is *USB1)

    b. Speed: 115200
2. Press reset button (Note: The Nios V needs some seconds to load the software project from the flash memory)
3. Console output depends on used Software project, see Software Design - SDK#Application

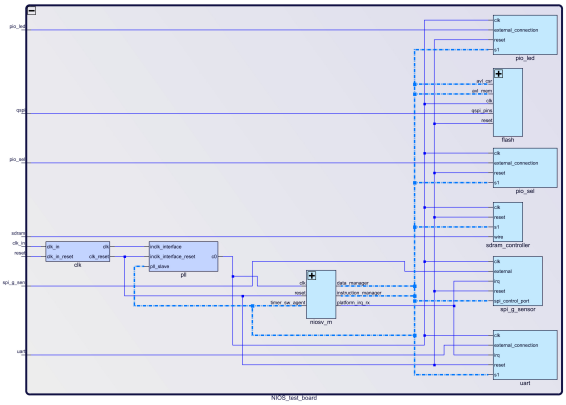
System Design - Quartus

Block Design

The block designs may differ depending on the assembly variant.



Block Design - Project



Block Design - Platform Designer

Software Design - SDK

Application

Used software project depends on board assembly variant. Template location: *<project folder> /source_files/software/*

test_tei0001

Software example to test TEI0001 module.

- You can toggle between following modes by pressing user button
    1. Spirit level
    2. Pulse-width modulation sequence
    3. Shift register sequence
    4. Knightrider sequence
    5. Case statement sequence

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String,	• update to Quartus Prime Lite 22.1

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian

.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	.user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2022-06-15	v.16	Thomas Dück	• update to Quartus Prime Lite 21.1
2021-07-09	v.14	Thomas Dück	• update to Quartus Prime Lite 20.1 • document style update • script update
2020-10-09	v.12	Thomas Dück	• bugfixes • script update
2020-05-13	v.10	Thomas Dück	• 19.1 release
2019-11-11	v.8	Thomas Dück	• add bash files for Linux OS
2019-10-29	v.6	Thomas Dück	• change design to TE scripts • new variants
2019-04-03	v.4	Thomas Dück	• Initial release 18.1
--	all		--

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy24.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page]

due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.

		atlassian . confluence.core. ContentEntityObject]	

Document change history.

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]