# TEBT0808 TRM

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**Table of Contents**

# Overview

The Trenz Electronic TEBT0808 is a test fixture for module TE0808(REV02, REV03) and TE0803(REV01) series.

Refer to http://trenz.org/tebt0808-info for the current online version of this manual and other available documentation.

# Key Features

- **Modules**
    - TE0808, TE0803

- **On Board**
  - ○ Done/Error/Status LEDs
  - ○ MEMS Oscillator 125.00 MHz
  - ○ Boot Mode DIP-Switch
  - ○ 2x DIP-Switches to control TE080x power domains
- **Interface**
  - ○ Pin Header for TE0790 JTAG/UART Adapter
  - ○ ARM JTAG header
  - ○ Pin Header for I$^2$C
  - ○ Board to Board (B2B) Connectors
  - ○ One PL GT with 4x SMA Connectors
  - ○ One PS GT with 4x SMA Connectors
  - ○ One pre-assembled TE0790 XMOD FTDI JTAG adapter
- **Power:**
  - ○ 3.3 V (Nominal Supply Voltage)
- **Dimension:** 90mm x 90mm

## Block Diagram

### TEBT0808
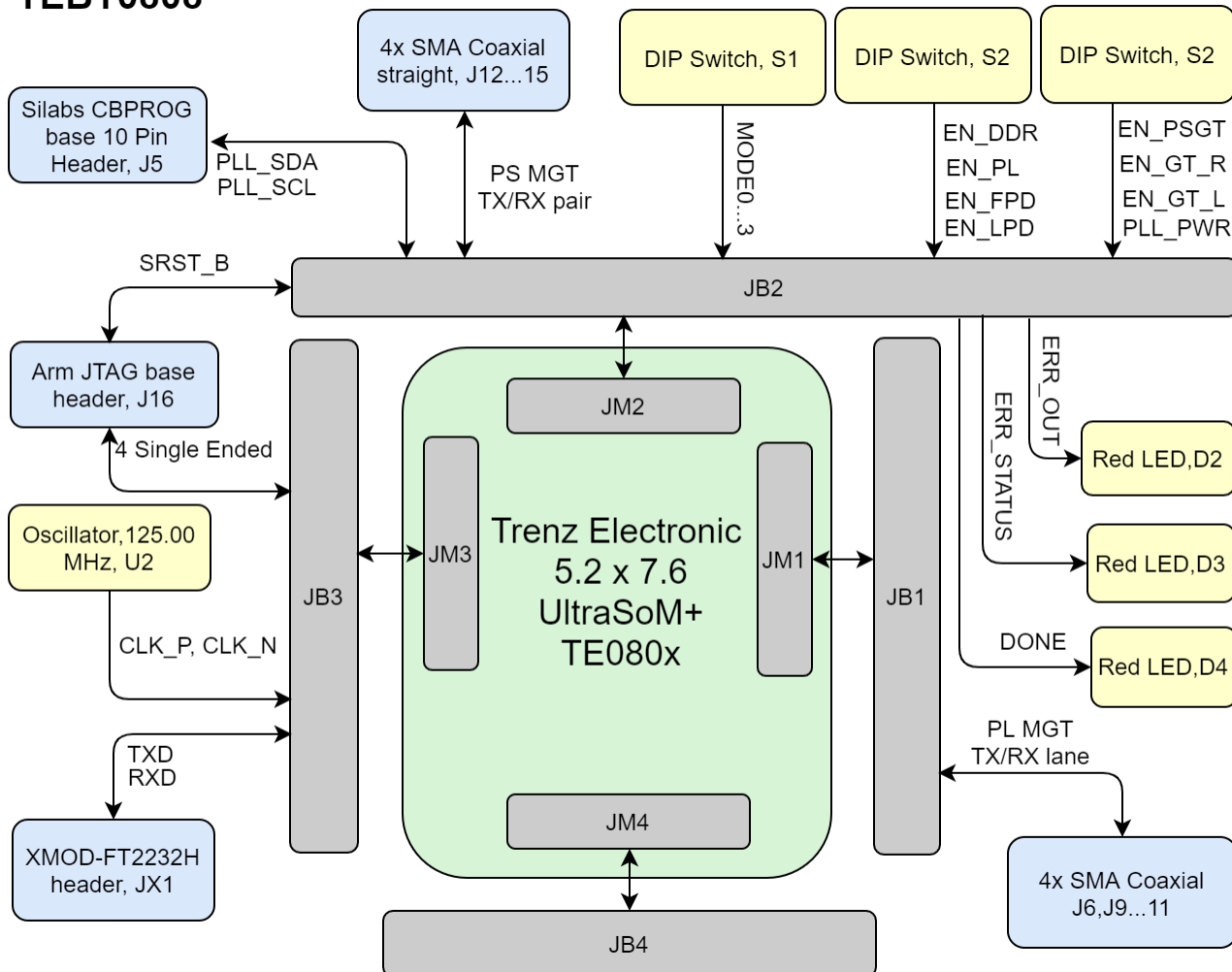


**TEBT0808 Block Diagram**

# Main Components
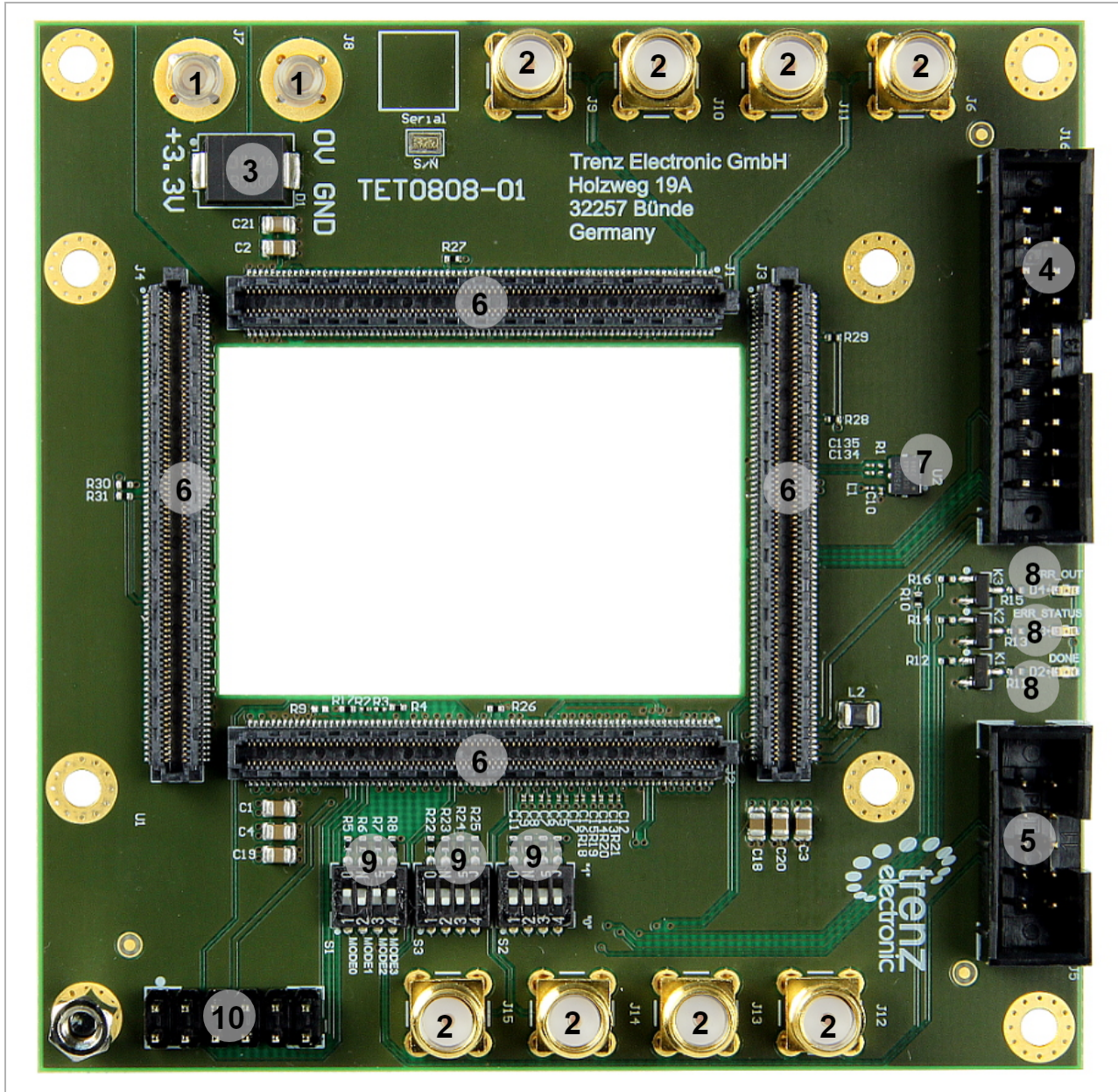


**TEBT0808 Main Components**

1. Uninsulated Power Jack. J7-J8
2. SMA Coaxial straight. J6- J9...15
3. Surface Mount Schottky Barrier Rectifier. D1
4. ARM PJTAG Pin Header J16
5. I2C Pin Header, J5
6. Board to Board Connectors. J1...4
7. MEMS Oscillator, U2
8. On-Board LEDs, D2...4

9. DIP-Switch, S1...3
10. XMOD header, JX1

## Initial Delivery State

| Storage device name | Content | Notes |
|---|---|---|
| - | - | - |

**Initial delivery state of programmable devices on the module**

## Configuration Signals

Boot mode can be set by DIP-Switch S1.

| M3 | M2 | M1 | M0 | Bootmode | Bootmode | Notes |
|---|---|---|---|---|---|---|
| ON | ON | ON | ON | 0b0000 | PS Main JTAG (TE0790 USB JTAG) | DIPs are inverted |
| ON | ON | OFF | ON | 0b0010 | SPI Flash (dual parallel, 4bit x 2, 32bit Addressing) | DIPs are inverted |
| OFF | ON | ON | ON | 0b1000 | PJTAG(MIO29:26) | DIPs are inverted |

**Boot Process.**

| Signal | B2B | Note |
|---|---|---|
| PLL_RST | J2-89 | |
| SRST_B | J2-96 | Connected to PJTAG0_SRST - J16 |

**Reset Process.**

# Signals, Interfaces and Pins

## Board to Board (B2B) I/Os

TEBT0808 has four B2B Connectors and each connector has 160 pins. Number of I/O signals and Interfaces connected to the B2B connectors is as following table:

| B2B Connector | Interfaces | Number of I/O | Notes |
|---|---|---|---|

| | | | |
|---|---|---|---|
| J1 | User I/O | 46 Single Ended, 23 Differential | IOs are Loop-Back |
| | | | IOs are Loop-Back |
| | | 16 Single Ended, 8 Differential | IOs are Loop-Back |
| | | | IOs are Loop-Back |
| | | 16 Single Ended, 8 Differential | PL_1V8 |
| | | 16 Single Ended, 8 Differential | |
| | | 4 Single Ended | |
| J2 | User IO | 28 Single Ended, 14 Differential | IOs are Loop-Back |
| | | | IOs are Loop-Back |
| | | 6 Single Ended, 3 Differential | |
| | Boot Mode | 4 Single Ended | MODE0...3 |
| | Control Signals | 25 Single Ended | PLL_SEL0, PLL_SEL1, PLL_RST, EN_GTR, EN_PL, PLL_LOLN, EN_PSGT, ERR_STATUS, ERR_OUT,SRST_B, INIT_B, PROG_B, EN_FPD , EN_LPD , DONE, EN_PLL_PWR, PLL_FINC ,PG_PLL_1V8, LP_GOOD, PG_DDR, PG_PL, PG_FPD, PG_PSGT, PG_GT_R, PG_GT_L |
| | JTAG Interface | 7 Single Ended | TCK, TDI, TMS, TDO, MR, Rxd, Txd |
| | I$^2$C | 2 Single Ended | PLL_SCL, PLL_SDA |
| | Clock | 6 Single Ended, 3 Differential | CLK0, CLK7, CLK8 |
| J3 | User IO | 24 Single Ended, 12 Differential | Connected to Module FPGA, Bank 48 |
| | | | Connected to Module FPGA, Bank 47 |
| | | 24 Single Ended, 12 Differential | |
| | Clock | 6 Single Ended, 3 Differential | CLK228, CLK229, CLK230 |
| | PJTAG Interface | 4 Single Ended | PJTAG0_TCK, PJTAG0_TDI, PJTAG0_TMS, PJTAG0_TDO, |
| | MIO | 45 Single Ended | MIO13..77 |
| | UART | 2 Single Ended | TXD, RXD |
| | Power Control Signals | 4 Single Ended | PS_1V8, SI_PLL_1V8, VCCO_48, VCCO_47, PLL_3V3 |

| | | 48 Single Ended, 24 Differential | IOs are Loop-Back |
| J4 | User I/O | | IOs are Loop-Back |
| | | 48 Single Ended, 24 Differential | B64_T0...3 |
| | | | B65_T0...3 |
| | | 4 Single Ended | |
| | | 4 Single Ended | |
| | Power pins | 4 Single Ended | VCCO_64, VCCO65 |

**General PL I/O to B2B connectors information**

# SMA Coaxial Connectors

TEBT0808 is equipped with 8 SMD Coaxial Connectors.

| Designator | Schematic | B2B Connector | Notes |
|---|---|---|---|
| J6 | B230_TX3_P | J1 | |
| J9 | B230_RX3_N | J1 | |
| J10 | B230_RX3_P | J1 | |
| J11 | B230_TX3_P | J1 | |
| J12 | B505_TX0_N | J2 | |
| J13 | B5050TX0_P | J2 | |
| J14 | B505_RX0_N | J2 | |
| J15 | B505_RX0_P | J2 | |

**SMD Coaxial Connectors**

# XMOD JTAG

JTAG access to the TEBT080X  is available through B2B connector JB2 using XMOD adapter TE0790.

| JTAG Signal | B2B Connector | Notes |
|---|---|---|
| TMS | J2- 126 | |
| TDI | J2- 122 | |
| TDO | J2- 124 | |
| TCK | J2- 120 | |

**JTAG Pins Connection**

The voltages 3.3V (VCC) and VIO (variable SC CPLD I/O-voltage) on TE0790 can be configured by the DIP-switch S2 which must be set as following.

| DIP Switch,S2 | Default | Description |
|---|---|---|
| 1 | ON | Update Mode JTAG access to SC CPLD only |
| 2 | OFF | Must be always in OFF state. |

| 3 | OFF | VIO is supplied from Module |
|---|---|---|
| 4 | OFF | 3.3V is supplied by the carrier TEBT0808 |

**Xmod Adapter DIP-Switch Setting Description**

# PJTAG

PJTAG access to the TEBT0808 is available through B2B connector JB3.

| JTAG Signal | B2B Connector | Notes |
|---|---|---|
| PJTAG_TMS | J3- 94 | |
| PJTAG_TDI | J3- 90 | |
| PJTAG_TDO | J3- 92 | |
| PJTAG_TCK | J3- 88 | |
| PJTAG_SRST | J2- 96 | Connected to SRST_B |

**PJTAG Pins Connection**

# Pin header

The I2C signals can be accessed through pin header J5.

| Signals | B2B Connector | Pin Header | Notes |
|---|---|---|---|
| PLL_SCL | J2- 90 | J5- 3 | |
| PLL_SDA | J2- 92 | J5- 7 | |

**I2C Connections**

# Test Points

| Test Point | Signals | B2B Connector | Notes |
|---|---|---|---|
| TP 1 | DDR_1V2 | J2-135 | |
| TP 2 | PG_PSGT | J2-82 | |
| TP 3 | ERR_STATUS | J2-86 | |
| TP 4 | PLL_FDEC | J2-94 | |
| TP 5 | EN_LPD | J2-108 | |
| TP 6 | EN_DDR | J2-112 | |
| TP 7 | PG_PL | J2-104 | |
| TP 8 | PG_PLL_1V8 | J2-80 | |
| TP 9 | N_PSGT | J2-84 | |
| TP 10 | ERR_OUT | J2-88 | |
| TP 11 | EN_FPD | J2-102 | |
| TP 12 | LP_GOOD | J2-106 | |
| TP 13 | PG_FPD | J2-110 | |

| | | | |
|---|---|---|---|
| TP 14 | PG_DDR | J2-114 | |
| TP 15 | EN_PLL_PWR | J2-77 | |
| TP 16 | PLL_FINC | J2-81 | |
| TP 17 | PG_GT_R | J2-91 | |
| TP 18 | EN_GT_R | J2-95 | |
| TP 19 | EN_PL | J2-101 | |
| TP 20 | EN_GT_L | J2-79 | |
| TP 21 | PLL_SEL0 | J2-93 | |
| TP 22 | PG_GT_L | J2-97 | |
| TP 23 | INIT_B | J2-98 | |
| TP 24 | IN1_P | J2-4 | |
| TP 25 | PLL_SEL1 | J2-87 | |
| TP 26 | PLL_LOLN | J2-85 | |
| TP 27 | PLL_RST | J2-89 | |
| TP 28 | DX_P | J2-119 | |
| TP 29 | DX_N | J2-121 | |
| TP 30 | IN1_N | J2-6 | |
| TP 31 | B505_CLK0_P | J2-10 | |
| TP 32 | B505_CLK0_N | J2-12 | |
| TP 33 | B505_CLK1_P | J2-16 | |
| TP 34 | B505_CLK1_N | J2-18 | |
| TP 35 | B128_CLK1_P | J2-22 | |
| TP 36 | B128_CLK1_N | J2-24 | |
| TP 37 | CLK0_N | J2-1 | |
| TP 38 | CLK0_P | J2-3 | |
| TP 39 | CLK8_P | J2-7 | |
| TP 40 | CLK8_N | J2-9 | |
| TP 41 | CLK7_P | J2-13 | |
| TP 42 | CLK7_N | J2-15 | |
| TP 43 | IN2_P | J3-66 | |
| TP 44 | IN2_N | J3-68 | |
| TP 45 | B230_CLK1_N | J3-59 | |
| TP 46 | B230_CLK1_P | J3-61 | |
| TP 47 | B229_CLK0_N | J3-65 | |
| TP 48 | B229_CLK0_P | J3-67 | |
| TP 49 | PLL_3V3 | J3-152 | |
| TP 50 | GND | J3-155 | |
| TP 51 | PL_1V8 | J1-121 | |
| TP 52 | PS_1V8 | J3-147 | |
| TP 53 | SI_PLL_1V8 | J3-151 | |

| TP 54 | PROG_B | J2-100 | |
|---|---|---|---|
| TP 55...56 | GND | - | |

**Test Points Information**

# On-board Peripherals

| Chip/Interface | Designator | Notes |
|---|---|---|
| DIP Switch | S1...3 | |
| LEDs | D2...4 | Red LEDs |
| Oscillator | U2 | 125.00 MHz |

**On Board Peripherals**

## DIP Switch

There are three DIP Switches, S1, S2, S3.

The Boot Mode can be set through DIP Switch S1, refer to BootMode table.

| DIP Switch S1 | Signals | B2B | Notes |
|---|---|---|---|
| S1A | MODE0 | J2-109 | |
| S1B | MODE1 | J2-107 | |
| S1C | MODE2 | J2-105 | |
| S1D | MODE3 | J2-103 | |

**DIP Switch S1**

Control signals must be set using DIP Switch S2, S3.

| DIP Switch S2 | Signals | B2B | Notes |
|---|---|---|---|
| S2A | EN_PSGT | J2-84 | Position OFF enables power rail |
| S2B | EN_GT_R | J2-95 | Position OFF enables power rail |
| S2C | EN_GT_L | J2-97 | Position OFF enables power rail |
| S2D | EN_PLL_PWR | J2-77 | Position OFF enables power rail, connected to PG_PL |

**DIP Switch S2**

| DIP Switch S3 | Signals | B2B | S3 switch | Notes |
|---|---|---|---|---|
| S3A | EN_DDR | J2-112 | S3A | Position OFF enables power rail |
| S3B | EN_LPD | J2-108 | S3B | Position OFF enables power rail |
| S3C | EN_PL | J2-101 | S3C | Position OFF enables power rail |
| S3D | EN_FPD | J2-102 | S3D | Position OFF enables power rail |

**DIP Switch S3**

## LEDs

| Designator | Color | Connected to | Active Level | Note |
|---|---|---|---|---|
| D2 | Red | DONE | Active High | Non User LED |
| D3 | Red | ERR_STATUS | Active High | Non User LED |
| D4 | Red | ERR_OUT | Active High | Non User LED |

**On-board LEDs**

## Clock Sources

| Designator | Description | Frequency | Note |
|---|---|---|---|
| U2 | MEMS Oscillator | 125.00 MHz | |

**Osillators**

# Power and Power-On Sequence

## Power Supply

| 2,0mm MC LB2 | Note |
|---|---|
| J7 | 3.3V direct modules power supply |
| J8 | GND |

**Power Consumption**

## Power Consumption

Minimum current depends mainly on design and cooling solution. Use Xilinx Power Estimator and/or Your Vivado Project to estimate min current. Minimum of 3A are recommanded for basic functionality.
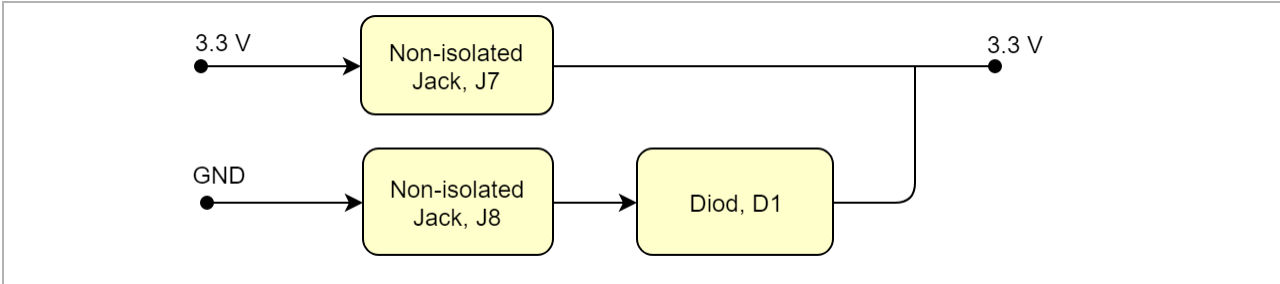
| Power Input Pin | Typical Current |
|---|---|
| 3.3V | TBD* |

**Power Consumption**

* TBD - To Be Determined

## Power Distribution Dependencies

Input oower sourced directly the module, Only one Diode D1 is used for inverse polarity protection.

**Power Distribution**

## Power Rails

| Power Rail Name | B2B J1 Pins | B2B J2 Pins | B2B J3 Pins | Directions | Note |
|---|---|---|---|---|---|
| PL_DCIN | 151, 153, 155, 157, 159 | - | - | Output | - |
| DCDCIN | - | 154, 156, 158, 160, 153, 155, 157, 159 | - | Output | - |
| LP_DCDC | - | 138, 140, 142, 144 | - | Output | - |
| PS_BATT | - | 125 | - | Output | - |
| GT_DCDC | - | - | 157, 158, 159, 160 | Output | - |
| PLL_3V3 | - | - | 152 | Output | - |
| SI_PLL_1V8 | - | - | 151 | Input | - |
| PS_1V8 | - | 99 | 147, 148 | Input | - |
| PL_1V8 | 91, 121 | - | - | Input | - |
| DDR_1V2 | - | 135 | - | Input | - |

**Module power rails.**

# Board to Board Connectors

5.2 x 7.6 cm UltraSoM+ modules use four Samtec Razor Beam LP Terminal Strip (ST5) on the bottom side.

- 4x REF-192552-02 (160-pins)
    - ST5 Mates with SS5

5.2 x 7.6 cm UltraSoM+ carrier use four Samtec Razor Beam LP Socket Strip (SS5) on the top side.

- 4x REF192552-01 (160-pins)
    - SS5 Mates with ST5

## Features

- Board-to-Board Connector 160-pins, 80 contacts per row
- Ultrafine .0197" (0.50 mm) pitch
- Narrow body design saves space on board
- Lead style -03.5
- Samtec 28+ Gbps Solution
- Mates with: ST5

- Insulator Material: Liquid Crystal Polymer, schwarz
- Operating Temperature Range: -55°C bis +125°C
- Lead-Free Solderable: Yes
- RoHS Konform: Yes

## Connector Stacking height

When using the standard type on baseboard and module, the mating height is 5 mm.

Other mating heights are possible by using connectors with a different height:

| Order number | REF number | Samtec Number | Type | Contribution to stacking height | Comment |
|---|---|---|---|---|---|
| 27219 | REF192552-01 | SS5-80-3.50-L-D-K-TR | Baseboard connector | 3.5mm | Standard connector used on carrier |
| 27018 | REF-189545-02 | SS5-80-3.00-L-D-K-TR | Baseboard connector | 3 mm | Assembly option on request |
| 27220 | REF-192552-02 | ST5-80-1.50-L-D-P-TR | Module connector | 1.5 mm | Standard connector used on modules |
| 27017 | REF-189545-01 | ST5-80-1.00-L-D-P-TR | Module connector | 1 mm | Assembly option on request |

**Connectors.**

The module can be manufactured using other connectors upon request.

## Current Rating

Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

## Connector Speed Ratings

The connector speed rating depends on the stacking height:

| Stacking height | Speed rating |
|---|---|
| 4 mm, Single-Ended | 13GHz/26Gbps |
| 4 mm, Differential | 13.5GHz/27Gbps |
| 5 mm, Single-Ended | 13.5GHz/27Gbps |
| 5 mm, Differential | 20GHz/40 Gbps |

**Speed rating.**

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

## Manufacturer Documentation

| File | Modified |
|---|---|
| PDF File hsc-report-sma_st5-ss5-04mm_web.pdf | 30 05, 2017 by Susanne Kunath |
| PDF File hsc-report-sma_st5-ss5-05mm_web.pdf | 30 05, 2017 by Susanne Kunath |
| PDF File REF-192552-01.pdf | 13 11, 2017 by John Hartfiel |

| PDF File REF-192552-02.pdf | 13 11, 2017 by John Hartfiel |
|---|---|
| PDF File ss5.pdf | 13 11, 2017 by John Hartfiel |
| PDF File ss5-st5.pdf | 13 11, 2017 by John Hartfiel |
| PDF File ss5-xx-x.xx-x-d-k-tr-mkt.pdf | 13 11, 2017 by John Hartfiel |
| PDF File st5.pdf | 13 11, 2017 by John Hartfiel |
| PDF File st5-xx-x.xx-x-d-p-tr-mkt.pdf | 13 11, 2017 by John Hartfiel |

Download All

# Technical Specifications

## Absolute Maximum Ratings

| Symbols | Min | Max | Unit | Note |
|---|---|---|---|---|
| VIN | -0.3 | 4 | V | VIN is connected directly to module |
| Storage Temperatur | -40 | +85 | °C | See DIP Switch, CHS-04TA datasheet |

**PS absolute maximum ratings**

## Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

| Symbols | Min | Max | Unit | Note |
|---|---|---|---|---|
| VIN | 3,14 | 3.47 | V | Check also TRM of the connected module |
| Operating Temperatur | -40 | +85 | °C | |

**Recommended operating conditions.**

## Physical Dimensions

- Module size: 90 mm × 90 mm.  Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 3.5 mm.

PCB thickness: 1.6 mm.
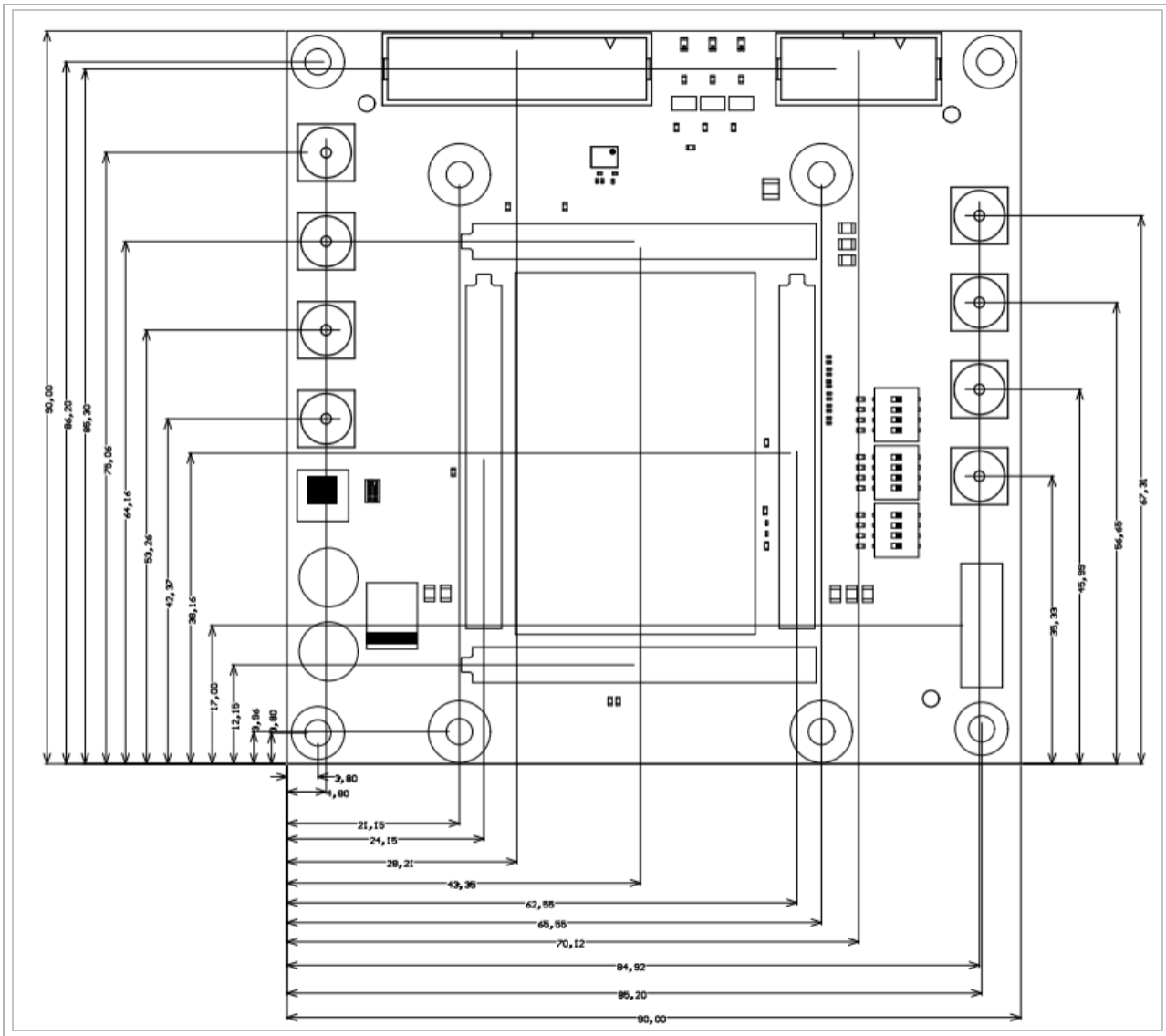
**Physical Dimension**

# Currently Offered Variants

| Trenz shop TEBT0808 overview page | |
|---|---|
| English page | German page |

**Trenz Electronic Shop Overview**

# Revision History

# Hardware Revision History

| Date | Revision | Changes | Documentation Link |
|------|----------|---------|-------------------|
| 2016-05-30 | 01 | Initial Release | REV01 |

**Hardware Revision History**

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.
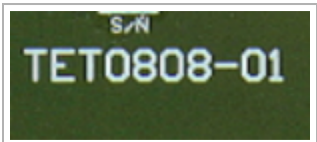


**Board hardware revision number.**

# Document Change History

| Date | Revision | Contributor | Description |
|------|----------|-------------|-------------|

| | | | Updated block diagram |
|---|---|---|---|
| **Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasCon tentLevelPermission. Cannot resolve which method to invoke for [null, class java. lang.String, class com. atlassian.confluence.pages. Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core. ContentEntityObject] | **Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasCon tentLevelPermission. Cannot resolve which method to invoke for [null, class java. lang.String, class com. atlassian.confluence.pages. Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core. ContentEntityObject] | **Error rendering macro 'page-info'** Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasCon tentLevelPermission. Cannot resolve which method to invoke for [null, class java. lang.String, class com. atlassian.confluence.pages. Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com. atlassian.confluence.core. ContentEntityObject] | |
| 2020-05-11 | v.54 | John Hartfiel | • add notes to DIP section • Correctio n on configura tion signal section |
| 2020-01-24 | v.49 | Pedram Babakhani | • Initial Release |

| -- | all | Edit | • -- |
|---|---|---|---|
| | | **Error rendering macro 'page-info'**<br><br>Ambiguous method overloading for method jdk. proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java. lang.String, class com. atlassian.confluence.pages. Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user. ConfluenceUser, class java. lang.String, class com. atlassian.confluence.core. ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com. atlassian.confluence.core. ContentEntityObject] | |

**Document change history.**

# Disclaimer

## Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

**Error rendering macro 'page-info'**

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]