

# TE0803 Test Board

## Table of contents

1 Overview

2 Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via Vitis.

3 Refer to <http://trenz-electronic.com/te0803-info> for the current online version of this manual and other available documentation.

1.1 Key Features

1.2 Revision History

1.3 Release Notes and Know Issues

1.4 Requirements

## Key Features

- Vitis/Vivado 2022.2
- QSPI
- Custom Carrier (minimum PS Setup)
- 2 Module BTL (some additional outputs only)
- 3 Launch
  - 3.1 Programming
    - 3.1.1 Get prebuilt boot binaries
    - 3.1.2 QSPI-Boot mode
    - 3.1.3 SD-Boot mode
    - 3.1.4 JTAG
  - 3.2 Usage

## Revision History

Date	Project Built	Authors	Description
2023-09-14	TE0803-test_board-vivado_2022.2-build_8_20230914124756.zip	Manuela Strücker	<ul style="list-style-type: none"><li>• 2022.2 update</li><li>• new assembly variants</li></ul>
2022-10-17	TE0803-test_board-vivado_2021.2-build_18_20221017093148.zip	Manuela Strücker	<ul style="list-style-type: none"><li>• script update</li></ul>
2022-08-30	TE0803-test_board-vivado_2021.2-build_15_20220830131430.zip	Manuela Strücker	<ul style="list-style-type: none"><li>• new assembly variants</li></ul>
2022-04-05	TE0803-test_board-vivado_2021.2-build_11_20220405100116.zip	Manuela Strücker	<ul style="list-style-type: none"><li>• 2021.2 update</li></ul>

2021-09-06	2020.2	TE0803-test_board-vivado_2020.2-build_7_20210906104518.zip TE0803-test_board_noprebui-lt-vivado_2020.2-build_7_20210906104536.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• 2020.2 update</li> <li>• update document style</li> </ul>
2020-04-06	2019.2	TE0803-test_board-vivado_2019.2-build_9_20200406081019.zip  TE0803-test_board_noprebui-lt-vivado_2019.2-build_9_20200406081036.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2020-03-25	2019.2	TE0803-test_board-vivado_2019.2-build_8_20200325082253.zip  TE0803-test_board_noprebui-lt-vivado_2019.2-build_8_20200325082311.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• script update</li> </ul>
2020-01-23	2019-2	TE0803-test_board-vivado_2019.2-build_3_20200123070036.zip  TE0803-test_board_noprebui-lt-vivado_2019.2-build_3_20200123070049.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• 2019.2 update</li> <li>• Vitis support</li> <li>• FSBL SI programming procedure update</li> </ul>
2019-5-06	2018.3	TE0803-test_board_noprebui-lt-vivado_2018.3-build_05_20190506161948.zip  TE0803-test_board-vivado_2018.3-build_05_20190506161936.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• custom FSBL</li> <li>• new assembly variants</li> </ul>
2018-10-26	2018.2	TE0803-test_board_noprebui-lt-vivado_2018.2-build_03_20181026141705.zip  TE0803-test_board-vivado_2018.2-build_03_20181026141651.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-08-14	2018.2	TE0803-test_board_noprebui-lt-vivado_2018.2-build_02_20180814103119.zip  TE0803-test_board-vivado_2018.2-build_02_20180814103105.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>

2018-07-13	2018.2	TE0803-test_board_noprebui lt-vivado_2018.2- build_02_20180713 085721.zip  TE0803-test_board- vivado_2018.2- build_02_20180713 085704.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• additional notes for FSBL generated with Win SDK</li> <li>• changed *.bif</li> </ul>
2018-05-17	2017.4	TE0803-test_board_noprebui lt-vivado_2017.4- build_09_20180517 152118.zip  TE0803-test_board- vivado_2017.4- build_09_20180517 152103.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-04-11	2017.4	TE0803-test_board_noprebui lt-vivado_2017.4- build_07_20180411 081821.zip  TE0803-test_board- vivado_2017.4- build_07_20180411 081757.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix TE0803-01-04EG board part file</li> </ul>
2018-02-13	2017.4	TE0803-test_board_noprebui lt-vivado_2017.4- build_06_20180213 120257.zip  TE0803-test_board- vivado_2017.4- build_06_20180213 120229.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-02-05	2017.4	TE0803-test_board- vivado_2017.4- build_05_20180205 101915.zip  TE0803-test_board_noprebui lt-vivado_2017.4- build_05_20180205 101943.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-01-31	2017.4	TE0803-test_board- vivado_2017.4- build_05_20180131 124202.zip  TE0803-test_board_noprebui lt-vivado_2017.4- build_05_20180131 124215.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-01-18	2017.4	TE0803-test_board- vivado_2017.4- build_05_20180118 160549.zip  TE0803-test_board_noprebui lt-vivado_2017.4- build_05_20180118 160604.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• rework Board Part Files</li> </ul>

2017-11-16	2017.2	TE0803-test_board-vivado_2017.2-build_05_20171116152716.zip  TE0803-test_board_noprebuilt-vivado_2017.2-build_05_20171116154619.zip	John Hartfiel	<ul style="list-style-type: none"> <li>Update Board Part CSV File with new Flash assembly variants</li> </ul>
2017-11-14	2017.2	TE0803-test_board-vivado_2017.2-build_05_20171114090712.zip  TE0803-test_board_noprebuilt-vivado_2017.2-build_05_20171114090725.zip	John Hartfiel	<ul style="list-style-type: none"> <li>Initial release</li> </ul>

**Design Revision History**

## Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see <a href="#">Xilinx Forum Request</a>	use corresponding board files for the Vivado versions	--
QSPI Flash	Flash programming is not supported with boot mode QSPI or SD.	If flash programming fails, configure device for JTAG boot mode and try again or use older Vivado Versions for programming. (Vivado 2020.2 or 2019.2)	--

**Known Issues**

## Requirements

### Software

Software	Version	Note
Vitis	2022.2	needed, Vivado is included into Vitis installation

**Software**

### Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on "<project folder>\board\_files\\*\_board\_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0803-01-02EG-1E	2eg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-02CG-1E	2cg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-03EG-1E	3eg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-03CG-1E	3cg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-02EG-1EA	2eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-02CG-1EA	2cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-03EG-1EA	3eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-03CG-1EA	3cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-03EG-1EB	3eg_4gb	REV02 REV01	4GB	128MB	NA	NA	NA
TE0803-01-04CG-1EA	4cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-04EV-1EA	4ev_2gb	REV02 REV01	2GB	128MB	NA	NA	NA
TE0803-01-04EV-1E3	4ev_2gb	REV01	2GB	128MB	NA	1 mm connectors	NA
TE0803-01-04EG-1EA	4eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04CG-1EB	4cg_2gb	REV01	2GB	256MB	NA	NA	NA
TE0803-01-05EV-1EA	5ev_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-05EV-1IA	5ev_i_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-04EV-1E3	4ev_4gb	REV02	4GB	128MB	NA	1 mm connectors	NA
TE0803-02-04EG-1E3	4eg_4gb	REV02	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-2AE11-A	2cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-2BE11-A	2eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-3AE11-A	3cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-3BE11-A	3eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4AE11-A	4cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4BE11-A	4eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4BE21-L	4eg_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4BI21-A	4eg_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-4DE11-A	4ev_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4DE21-L	4ev_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA

TE0803-03-4GE21-L	4eg_2_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-5DE11-A	5ev_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-5DI21-A	5ev_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-3RI21-A	3eg_li_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-3BI21-A	3eg_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-4DI21-L	4ev_i_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4GI11-A	4eg_2i_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4GE11-A	4eg_2_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4GI21-A	4eg_2i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-5BE11-A	5eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-5DI24-A	5ev_i_4gb	REV03	4GB	512MB	NA	NA	NA
TE0803-03-4BI21-X	4eg_i_4gb	REV03	4GB	128MB	NA	NA	U41 replaced with diode
TE0803-03-3BE21-A	3eg_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-3BE31-A*	3eg_8gb	REV03	8GB	128MB	NA	NA	dual die ddr
TE0803-04-2AE11-A	2cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-2BE11-A	2eg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-3AE11-A	3cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-3BE11-A	3eg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-4BE21-L	4eg_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0803-04-4BI21-A	4eg_i_4gb	REV04	4GB	128MB	NA	NA	NA
TE0803-04-4BI21-X	4eg_i_4gb	REV04	4GB	128MB	NA	NA	U41 replaced with diode
TE0803-03-4BI61-A	4eg_8gb	REV03	8GB	128MB	NA	NA	dual die ddr
TE0803-03-4BI61-X	4eg_8gb	REV03	8GB	128MB	NA	NA	dual die ddr
TE0803-04-4BI61-A	4eg_8gb	REV04	8GB	128MB	NA	NA	dual die ddr
TE0803-04-4BI61-X	4eg_8gb	REV04	8GB	128MB	NA	NA	dual die ddr
TE0803-04-4DE11-A	4ev_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-4DE21-L	4ev_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0803-04-4DI21-L	4ev_i_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4DI21-D	4ev_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-04-4DI21-D	4ev_i_4gb	REV04	4GB	128MB	NA	NA	NA

TE0803-04-4GE21-L	4eg_2_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0803-04-4GI21-A	4eg_2i_4gb	REV04	4GB	128MB	NA	NA	NA
TE0803-04-5BE11-A	5eg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-5DE11-A	5ev_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-5DI21-A	5ev_i_4gb	REV04	4GB	128MB	NA	NA	NA
TE0803-03-S003	4ev_2gb	REV04	2GB	128MB	NA	NA	CAO
TE0803-03-S006	4ev_4gb	REV04	4GB	128MB	NA	1 mm connectors	CAO
TE0803-04-4BE11-A	4eg_2gb	REV04	2GB	128MB	NA	NA	CAO
TE0803-03-S005	4eg_2gb	REV03	2GB	128MB	NA	NA	CAO: TE0803-03-4BI17-A
TE0803-04-S009	4eg_2_4gb	REV04	4GB	128MB	NA	1 mm connectors	CAO: TE0803-04-4GE21-L
TE0803-04-S011	4eg_2_4gb	REV04	4GB	64MB	NA	1 mm connectors	CAO: TE0803-04-4GE25-L
TE0803-04-4AE11-A	4cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S012	2cg_2gb	REV04	2GB	128MB	NA	NA	CAO
TE0803-03-4DE21-LZ	4ev_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-3AE11-AK	3cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-04-4AE11-AK	4cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-4DE11-AZ	4ev_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S013	3cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S014	4eg_2_4gb	REV04	4GB	64MB	NA	1 mm connectors	CAO: TE0803-04-4GE27-LZ
TE0803-04-S016	4cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S017	2eg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S018	4eg_2_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0803-04-S020	4cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-3BE21-L	3eg_4gb	REV04	4GB	128MB	NA	NA	NA
TE0803-04-4AE11-AZ	4cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-4DE21-LZ	4ev_4gb	REV04	4GB	128MB	NA	1 mm connectors	NA
TE0803-04-3AE11-AK	3cg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S022	4eg_2_4gb	REV04	4GB	128MB	NA	1 mm connectors	CAO: TE0803-04-4GE21-LZ

TE0803-04-S023	4eg_2_4gb	REV04	4GB	128MB	NA	1 mm connectors	CAO: TE0803-04-4GE81-L
TE0803-04-4BE11-AK	4eg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S026	5ev_i_4gb	REV04	4GB	128MB	NA	NA	CAO: TE0803-04-5DI21-A
TE0803-04-2BE11-AK	2eg_2gb	REV04	2GB	128MB	NA	NA	NA
TE0803-04-S010	5ev_2gb	REV04	2GB	128MB	NA	NA	CAO: TE0803-04-5DE11-A

\*used as reference

### Hardware Modules

Note: Design contains also Board Part Files for TE0803+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808*	Used as reference carrier. <b>Important:</b> CPLD Firmware REV07 or newer is recommended
TEBT0808-01	Change UART0 to UART1 (MIO68...69) and regenerate design

\*used as reference

### Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
---	---

\*used as reference

### Additional Hardware

## Content

For general structure and usage of the reference design, see [Project Delivery - AMD devices](#)

## Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts



Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
-------	-------------------------	---

#### Design sources

## Additional Sources

Type	Location	Notes
---	---	---

#### Additional design sources

## Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado <a href="#">hardware description file</a> for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

#### Prebuilt files (only on ZIP with prebuilt content)

## Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0803 "Test Board" Reference Design](#)

## Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery](#).

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)



**Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

#### **\_create\_win\_setup.cmd/\_create\_linux\_setup.sh**

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference
Design-----
-----
-- (0) Module selection guide, project creation...prebuilt export...
-- (1) Create minimum setup of CMD-Files and exit Batch
-- (2) Create maximum setup of CMD-Files and exit Batch
-- (3) (internal only) Dev
-- (4) (internal only) Prod
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (g) Install Board Files from Xilinx Board Store (beta)
-- (a) Start design with unsupported Vivado Version (beta)
-- (x) Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
  - optional for manual changes: Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_gui mode.cmd"




Note: Select correct one, see also [Vivado Board Part Flow](#)

**Important:** Use Board Part Files, which **did not** ends with \*\_tebf0808

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

**run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")**


```
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.

#### 5. Generate Programming Files with Vitis


**run on Vivado TCL (Script generates applications and bootable files, which are defined in "test\_board\sw\_lib\apps\_list.csv")**

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start
with TE Scripts on Vivado TCL)
```

 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)

## Launch


## Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design.  
Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)

## Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select create and open delivery binary folder

 Note: Folder "<project folder>\\_binaries\_<Article Name>" with subfolder "boot\_<app name>" for different applications will be generated

## QSPI-Boot mode

1. Connect **JTAG** and power on carrier with module

2. Open Vivado Project with "vivado\_open\_existing\_project\_gui mode.cmd" or if not created, create with "vivado\_create\_project\_gui mode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp hello_te0803
```

## SD-Boot mode

This does not work, because SD controller is not selected on PS.

## JTAG

Load configuration and Application with Vitis Debugger into device

## Usage

QSPI Boot:

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode



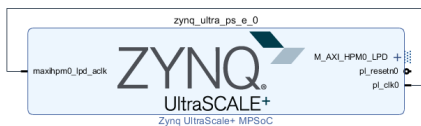
Note: See TRM of the Carrier, which is used.

4. Power On PCB

1. ZynqMP Boot ROM loads FSBL from QSPI into OCM,
2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from QSPI into DDR,

## System Design - Vivado

## Block Design



Block Design

## PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected UART to second controller or other MIO
SWDT0..1	
TTC0..3	

#### PS Interfaces

## Constrains

### Basic module constrains

<b>_i_bitgen.xdc</b>
<pre>set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design] set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]</pre>

### Design specific constrain

Not needed.

## Software Design - Vitis

For Vitis project creation, follow instructions from:

[Vitis](#)

## Application

Template location: "<project folder>\sw\_lib\sw\_apps\"

### zynqmp\_fsbl

TE modified 2022.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

## hello\_te0803

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

## Additional Software

No additional software is needed.

## Appx. A: Change History and Legal Notices

### Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
<div>Error renderi ng macro 'page- info'</div> <div>Ambiguo us method overload ing for method jdk. proxy27 9.\$Proxy 4022#ha sConten tLevelPe rmission . Cannot</div>	<div>Error renderi ng macro 'page- info'</div> <div>Ambiguo us method overload ing for method jdk. proxy27 9.\$Proxy 4022#ha sConten tLevelPe rmission . Cannot</div>	<div>Error renderi ng macro 'page- info'</div> <div>Ambiguo us method overload ing for method jdk. proxy27 9.\$Proxy 4022#ha sConten tLevelPe rmission . Cannot</div>	<div><ul style="list-style-type: none"><li>Release 2022.2</li><li>new assembly variants</li></ul></div>

resolve  
which  
method  
to  
invoke  
for [null,  
class  
java.  
lang.  
String,  
class  
com.  
atlassian  
.  
confluen  
ce.  
pages.  
Page]  
due to  
overlapp  
ing  
prototyp  
es  
between  
:  
[interfac  
e com.  
atlassian  
.  
confluen  
ce.user.  
Conflue  
nceUser  
, class  
java.  
lang.  
String,  
class  
com.

resolve  
which  
method  
to  
invoke  
for [null,  
class  
java.  
lang.  
String,  
class  
com.  
atlassian  
.  
confluen  
ce.  
pages.  
Page]  
due to  
overlapp  
ing  
prototyp  
es  
between  
:  
[interfac  
e com.  
atlassian  
.  
confluen  
ce.user.  
Conflue  
nceUser  
, class  
java.  
lang.  
String,  
class  
com.

resolve  
which  
method  
to  
invoke  
for [null,  
class  
java.  
lang.  
String,  
class  
com.  
atlassian  
.  
confluen  
ce.  
pages.  
Page]  
due to  
overlapp  
ing  
prototyp  
es  
between  
:  
[interfac  
e com.  
atlassian  
.  
confluen  
ce.user.  
Conflue  
nceUser  
, class  
java.  
lang.  
String,  
class  
com.

atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2022-10-17	v.33	Manuela Strücker	<ul style="list-style-type: none"> <li>script update</li> </ul>
2022-09-06	v.32	Manuela Strücker	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2022-07-15	v.30	Manuela Strücker	<ul style="list-style-type: none"> <li>Release 2021.2</li> </ul>
2021-09-09	v.25	Manuela Strücker	<ul style="list-style-type: none"> <li>Release 2020.2</li> </ul>
2020-04-06	v.24	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2020-03-25	v.23	John Hartfiel	<ul style="list-style-type: none"> <li>Script update</li> </ul>



2020-01-23	v.22	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2019.2</li> </ul>
2019-05-07	v.21	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2018.3</li> </ul>
2018-10-26	v.18	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-08-14	v.16	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-07-13	v.15	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2018.2</li> </ul>
2018-05-18	v.14	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-04-11	v.13	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix board part file</li> </ul>
2018-04-03	v.11	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-01-18	v.6	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2017.4</li> </ul>
2017-11-16	v.4	John Hartfiel	<ul style="list-style-type: none"> <li>• Update assembly versions with new Flash size</li> </ul>
2017-11-14	v.3	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2017.2</li> </ul>
	All	<div> Error  renderi  ng  macro  'page-  info'    Ambiguo  us  method  overload  ing for </div>	

method  
jdk.  
proxy27  
9.\$Proxy  
4022#ha  
sConten  
tLevelPe  
rmission  
.  
Cannot  
resolve  
which  
method  
to  
invoke  
for [null,  
class  
java.  
lang.  
String,  
class  
com.  
atlassian  
.  
confluen  
ce.  
pages.  
Page]  
due to  
overlapp  
ing  
prototyp  
es  
between  
:  
[interfac  
e com.  
atlassian  
.

		<div>confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]</div>	
--	--	--	--

Document change history.

## Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

## Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

## Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

## Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

## Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

## Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## REACH, RoHS and WEEE

### REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

### RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

## WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

### Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.

proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]