TE0705 CPLD Firmware

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TE0705 CPLD Access

Set S3-ENJTAG to OFF to get access to carrier CPLD.

Available CPLD Firmware

- TE0705 CPLD- Firmware description
 - Default delivered Firmware

Download

- TE0705/<PCB Revision>/Firmware/
 - O Use files from the subfolders of your PCB revision

General instructions

CPLD Firmware Update - General Requirements

- Lattice Diamond or Lattice Diamond Programmer is available for free on http://www.latticesemi.com/
- Lattice compatible JTAG Programmer, for example:
 - Trenz TE0790 or Carrier with FTDI for JTAG
 - $^{\circ}\,$ Most JTAG programmer, which used FTDI Chip to translate USB to JTAG
 - Digilent FTDI based programmer are not compatible with Lattice.
- JTAG must be connected to CPLD JTAG
- JTAG Enable Pin of CPLD must be selectable and set to VDD
- Correct CPLD Firmware (JED-File) from Trenz Electronic Download

CPLD Firmware Update - General Procedure

Important:

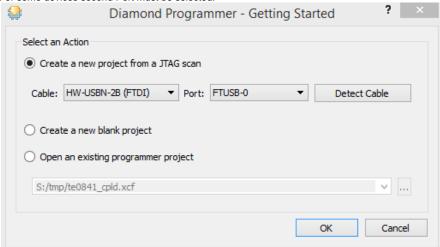
- · Connect only one JTAG device to host PC.
- Close all other JTAG programs, like Xilinx tools (on WinOS check hw_server.exe is terminated).

Procedure:

- 1. Enable CPLD JTAG access (See JTAG section on CPLD Firmware description)
- 2. Connect JTAG

- 3. Power on System
- 4. Open Lattice Diamond Programmer
- 5. Detect Cable and click "Ok"

For some devices second Port must be selected:



- 6. Select Device (See CPLD Firmware overview description). In the most cases select the correct detected device one time (it's yellow at first on the menue)
- 7. Select correct Firmware from Download Area (JED File)
- 8. Program CPLD: 9. Disable CPLD JTAG access (See JTAG section on CPLD Firmware description)
- 10. Restart System

More Information are available on the CPLD Firmware description and on the readme.txt included into the download zip.