TEI0009 TRM

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Overview

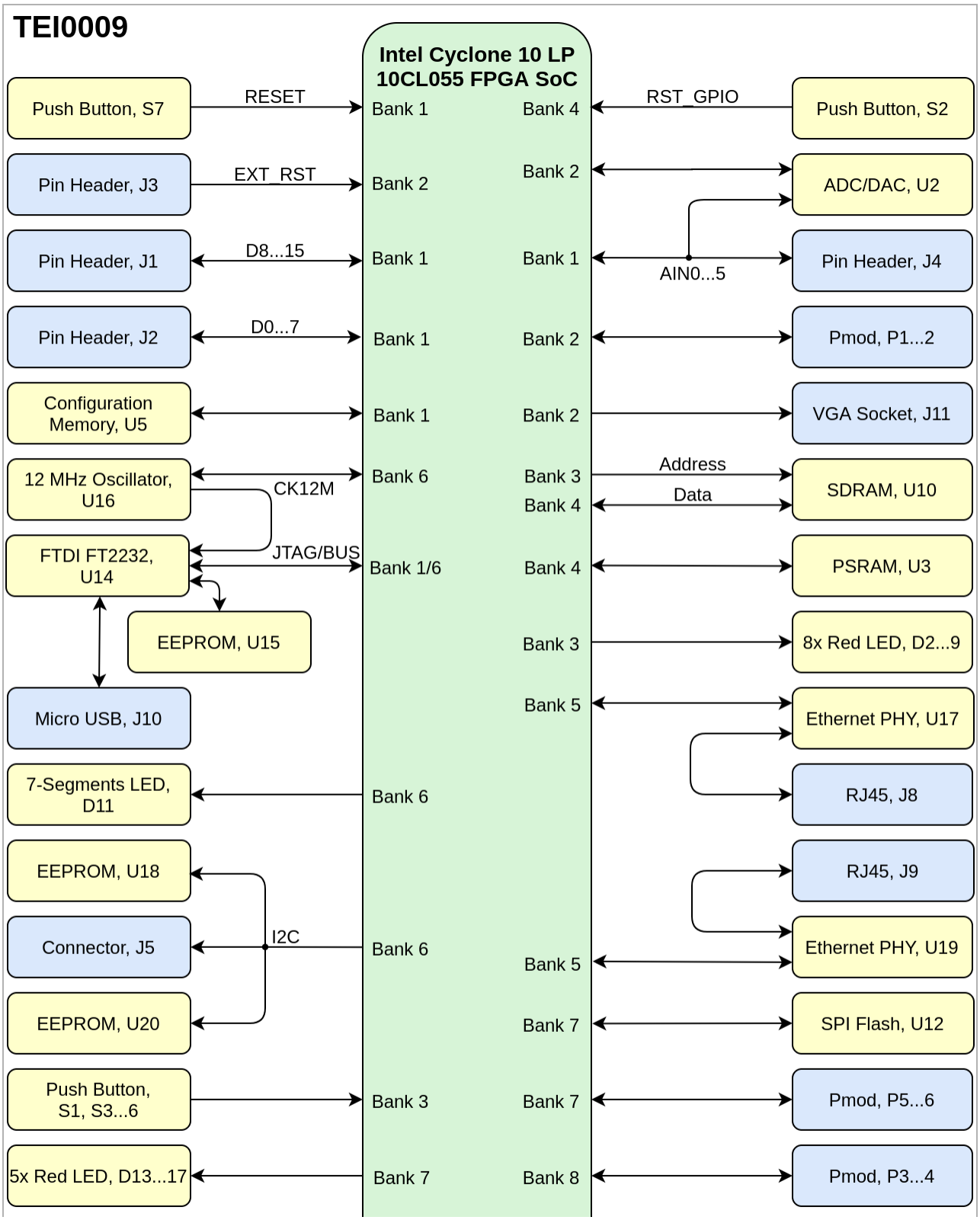
The Cyclone 10 LP Reference Kit is the world's first development board with a 55 kLE (Logic Elements) Intel Cyclone 10 LP and a variety of interfaces for numerous applications. The board is comprehensively tested and ready for use with end products and can also be ordered in customer-specific variants according to your requirements.

Refer to http://trenz.org/tei0009-info for the current online version of this manual and other available documentation.

Key Features

- Intel Cyclone 10 LP [10CL055YU484C8G]
  - Package: UBGA-484
  - Speed Grade: 8 (Slowest)
  - Temperature: 0 °C to 85° C
  - Package compatible device 10CL016, 10CL040, 10CL055, 10CL080 as assembly variant on request is possible
- 16 MBit (2 MByte) Flash Memory (optional up to 32 MBit (4 MByte))
- Integrated USB-JTAG Programmer
- Pin Header Connectors
- 64 MBit (8 MByte) SDRAM (optional up to 512 MBit (64 MByte))
- 64 MBit (8 MByte) User Quad-SPI Flash Memory (optional up to 128 MBit (16 MByte))
- 64 MBit (8 MByte) HyperRAM (Pseudo SRAM) (optional up to 128 MBit (16 MByte))
- 2x MAC Address EEPROM
- 2x Fast Ethernet PHY (10/100 Mbps)
- 8-Channel, 12-Bit, configurable ADC/DAC
- D-Sub Connector
- 2x RJ45 Connector
- LEDs:
  - Status LEDs, Power LED
  - 13x User LEDs
  - 7-Segment Display
- Push Buttons:
  - 2x Reset Push Buttons
  - 5x User Push Buttons
- I/O: 70 GPIO
- 5 V Power Supply
- Dimension: 95 mm x 110 mm
- Others:
  - Reverse Supply Protection
  - Undervoltage/Overvoltage Protection

Block Diagram


TEI0009
Intel Cyclone 10 LP
10CL055 FPGA SoC
Push Button, S7
RESET
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Bank 4
RST_GPIO
Push Button, S2
Pin Header, J3
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Bank 2
Bank 2
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Pin Header, J1
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Bank 1
Bank 1
AIN0...5
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Bank 2
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Bank 3
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Bank 6
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Bank 5
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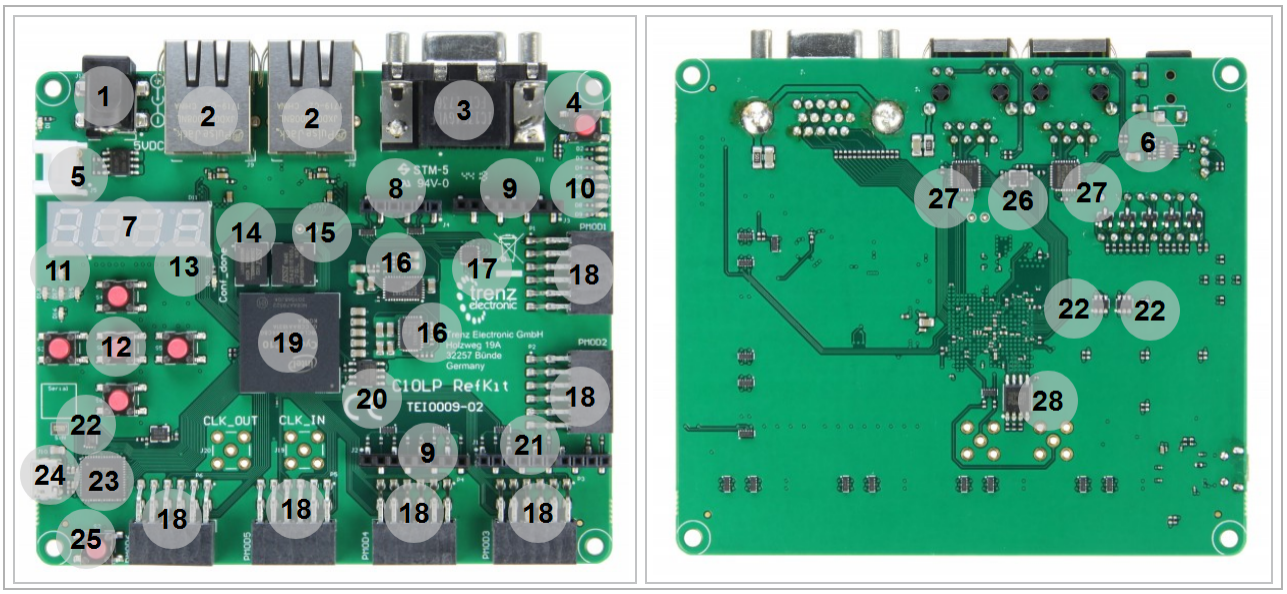
Bank 3
Bank 7
Pmod, P5...6
5x Red LED, D13...17
Bank 7
Bank 8
Pmod, P3...4

TEI0009 Block Diagram

Main Components



TEI0009 Main Components

1. Power Jack, J12
2. RJ45 Socket, J8...9
3. D-Sub Connector, J11
4. Push Button (Reset), S7
5. Grove Connector, J5
6. Undervoltage/Overvoltage Protector, U9
7. 7-Segment LED, D11
8. 1x6 Pin Header, J4
9. 1x8 Pin Header, J2...3
10. 8x User LEDs (Red), D2...9
11. 5x User LEDs (Red), D13...17
12. 5x User Push Buttons, S1 - S3...6
13. Red LED (CONF_DONE), D10
14. PSRAM Memory, U3
15. SDRAM Memory, U10
16. Voltage Regulator, U4 - U7
17. AD/DA Converter, U2
18. 6x Pmod Host Socket, P1...6
19. Intel Cyclone 10 LP, U1
20. Serial Configuration Memory, U5
21. 1x10 Pin Header, J1
22. EEPROM, U15 - U18 - U20
23. FTDI USB 2 to JTAG/UART Converter, U14
24. Micro USB 2.0, J10
25. Push Button (RST_GPIO), S2
26. Oscillator, U22
27. Ethernet PHY, U17 - U19
28. QSPI Flash Memory, U12

Initial Delivery State

Storage device name	Content	Notes
QSPI Flash (U12)	Not programmed	
EEPROM (U15)	Programmed	FTDI Configuration
EEPROM (U18, U20)	Not programmed	Except Ethernet MAC
SDRAM (U10)	Not programmed	
PSRAM (U3)	Not programmed	
Serial Configuration Memory (U5)	Programmed	

Initial Delivery State of Programmable Devices on the Module

Configuration Signals

Configuration mode has been set to AS (Active Serial) configuration.

MODE Signal State	MSEL0	MSEL1	MSEL2	MSEL3	Connected to	Boot Mode
MSEL[0:3]	0	1	0	0	Bank 6	AS (Active Serial)

Boot Process

Signal	Connected to	Note
RESET	S7, Push Button	Connected to nCONFIG.

Reset Process

Signals, Interfaces and Pins

I/Os on Pin Headers and Connectors

FPGA bank number and number of I/O signals connected to the connectors:

FPGA Bank	Connector	I/O Signal Count	Voltage Level	Notes
Bank 1	J1 (Pin header)	8 Single ended	3.3 V	
	J2 (Pin header)	8 Single ended	3.3 V	
	J4 (Pin header)	6 Single ended	3.3 V	
Bank 2	J3 (Pin header)	1 Single ended	3.3 V	
	P1 (Pmod Host Socket)	8 Single ended	3.3 V	
	P2 (Pmod Host Socket)	8 Single ended	3.3 V	
	J11 (VGA Host Socket)	14 Single ended	3.3 V	
Bank 6	J5 (Grove Connector)	2 Single ended	3.3 V	
Bank 7	P5 (Pmod Host Socket)	8 Single ended	3.3 V	
	P6 (Pmod Host Socket)	8 Single ended	3.3 V	

Bank 8	P3 (Pmod Host Socket)	8 Single ended	3.3 V	
	P4 (Pmod Host Socket)	8 Single ended	3.3 V	

General I/O to Pin Header and Pmod Connectors Information

Pmod Host Socket

TEI0009 has 6 Pmod 2x6 host sockets which are connected to Cyclon 10 LP (U1).

Designator	Signals	Connected to	Notes
P1	P1_IO1...8	Bank 2	
P2	P2_IO1...8	Bank 2	
P3	P3_IO1...8	Bank 8	
P4	P4_IO1...8	Bank 8	
P5	P5_IO1...8	Bank 7	
P6	P6_IO1...8	Bank 7	

Pmod SMD Host Socket Information

Pin Header

TEI0009 has 5 pin headers. The pin headers J1...4 are usable for Arduino modules, too.

Pin Header J1	Signals	Connected to	Notes
J1 - 1...6	D8...13	Bank 1	
J1 - 7	GND		
J1 - 8	AREF	ADC/DAC	
J1 - 9	D14_SDA	Bank 1	
J1 - 10	D14_SCL	Bank 1	

Pin Header J1

Pin Header J2	Signals	Connected to	Notes
J2 - 1	D0_RXD	Bank 1	
J2 - 2	D1_TXD	Bank 1	
J2 - 3...8	D2...4	Bank 1	

Pin Header J2

Pin Header J3	Signals	Connected to	Notes
J2 - 1	NC	-	
J3 - 2	3.3V	3.3 V	
J3 - 3	EXT_RST	Bank 2	Pulled-up to 3.3 V
J3 - 4	3.3V	3.3 V	
J3 - 5	5V	5 V	
J3 - 6...7	GND	GND	
J2 - 8	NC	-	

Pin Header J3

Pin Header J4	Signals	Connected to	Notes
J4 - 1...6	AIN0...5	FPGA Bank 1 and ADC/DAC	

Pin Header J4

Pin Header J5	Signals	Connected to	Notes
J5 - 1	I2C_SCL	FPGA Bank 6 and EEPROM (U18, U20)	Pulled-up to 3.3V.
J5 - 2	I2C_SDA	FPGA Bank 6 and EEPROM (U18, U20)	Pulled-up to 3.3V.
J5 - 3	3.3V	3.3 V	
J5 - 4	GND	GND	

Pin Header J5

Micro USB 2.0 Connector

FTDI FT2232 (U14) can be accessed through micro USB 2.0 B connector (J10) for JTAG (channel A). Channel B is connected to the FPGA and can be used for UART or other standards.

RJ45 Connectors

TEI0009 is equipped with two RJ45 connectors and two Ethernet PHYs. RJ45 connectors J8 and J9 are connected to Ethernet PHYs U17 and U19 respectively.

Pin	Schematic	ETH1 Pin	ETH2 Pin	Notes
TD+	ETH1_TX_P, ETH2_TX_P	U17 - TXP	U19 - TXP	
CT	ETH1_CTREF_TCT, ETH2_CTREF_TCT	-	-	
TD-	ETH1_TX_N, ETH2_TX_N	U17 - TXM	U19 - TXM	
RD+	ETH1_RX_P, ETH2_RX_P	U17 - RXP	U19 - RXP	
CT	ETH1_CTREF_RCT, ETH2_CTREF_RCT	-	-	
RD-	ETH1_RX_N, ETH2_RX_N	U17 - RXM	U19 - RXM	
LED Green	ETH1_LED0, ETH2_LED0	U17 - LED0/NWAYEN	U19 - LED0/NWAYEN	
LED Yellow	ETH1_LED1, ETH2_LED1	U17 - LED1/SPEED	U19 - LED1/SPEED	

RJ45 Connectors Information

D-Sub Connector

TEI0009 is equipped with a D-Sub connector which provides interface to Cyclone 10 LP through Bank 2.

Schematic	Corresponding Signals	Connected to	Notes
VGA_RED	VGA_R0...3	Bank 2	Red Channel
VGA_GREEN	VGA_G0...3	Bank 2	Green Channel
VGA_BLUE	VGA_B0...3	Bank 2	Blue Channel
VGA_RGB_HSYNC	VGA_HS	Bank 2	Horizontal Sync
VGA_RGB_VSYNC	VGA_VS	Bank 2	Vertical Sync

VGA Host Socket Information

On-board Peripherals

Chip/Interface	Designator	Notes
QSPI Flash Memory	U12	
SDRAM Memory	U10	
PSRAM Memory	U3	
7-Segment LED	D11	
FTDI FT2232	U14	
Ethernet PHY	U17, U19	
Serial Configuration Memory	U5	
ADC/DAC	U2	
EEPROM	U15, U18, U20	
User LEDs	D2...D10, D13...D17	
Push Buttons	S1...7	
Oscillators	U16, U22	

On-board Peripherals

QSPI Flash Memory

There is a 64 MBit (8 MByte) QSPI Flash memory (U12) provided by Integrated Silicon Solution Inc. which can be used to store data or configuration. Up to 128 MBit (16 MByte) memory is available on other assembly option.

Pin	Schematic	Connected to	Notes
CS	F_CS	Bank 7	
CLK	F_CLK	Bank 7	
IO0...3	F_IO0...3	Bank 7	

Quad SPI Interface MIOs and Pins

SDRAM Memory

The TEI0009 has 64 MBit (8 MByte) volatile memory provided by Integrated Silicon Solution Inc., SDRAM IC(U10) for storing user application code and data. Up to 512 MBit (64 MByte) SDRAM is available on other assembly option.

- Part number: IS42S16400J-7BL
- Supply voltage: 3.3 V
- Clock Frequency: 143 MHz (optional up to 200 MHz)
- Temperature: 0°C to 70°C (optional other ranges are available)

PSRAM Memory

The TEI0009 is integrated with 64 Mbit (8 MByte) Pseudo Static Random Access Memory (PSRAM) using a self-refresh DRAM array organized as 8M words by 8 bits. The device supports a HyperBus interface, Very Low Signal Count (Address, Command and data through 8 DQ pins), Hidden Refresh Operation, and Automotive Temperature Operation. Up to 128 MBit (16 MByte) memory is available on other assembly option.

- Part number: IS66WVH8M8
- Supply voltage: 3.3 V
- Clock Frequency: 100 MHz
- Temperature: -40°C to 85°C (optional other ranges are available)

7-Segment Display

The TEI0009 has a 4-Digit-7-Segment LED display which is connected to Bank 6.

Pin	Schematic	Connected to	Notes
A/L1	SEG_CA	Bank 6	
B/L2	SEG_CB	Bank 6	
C/L3	SEG_CC	Bank 6	
D	SEG_CD	Bank 6	
E	SEG_CE	Bank 6	
F	SEG_CF	Bank 6	
G	SEG_CG	Bank 6	
DP	SEG_CDP	Bank 6	
A1	SEG_AN	Bank 6	
A2	SEG_AN4	Bank 6	
A3	SEG_AN3	Bank 6	
A4	SEG_AN2	Bank 6	
L1-L3	SEG_AN1	Bank 6	

7-Segment LED Pins

FTDI FT2232

The FTDI chip U14 converts signals from USB 2.0 to a variety of standard serial and parallel interfaces. Refer to the FTDI data sheet for more information about the capacity of the FT2232H chip.
Channel A of FTDI FT2232H chip is used in MPPSE mode for JTAG. Channel B is routed to FPGA bank 6 and is usable for other standard interfaces.

The configuration of FTDI FT2232H chip is pre-programmed on the EEPROM U15.

FTDI Chip Pin	Signal Schematic Name	Connected to	Notes
ADBUS0	TCK	Bank 1	JTAG interface
ADBUS1	TDI	Bank 1	
ADBUS2	TDO	Bank 1	
ADBUS3	TMS	Bank 1	
BDBUS0...7	BDBUS0...7	Bank 6	
BCBUS0...7	BCBUS0...7	Bank 6	
EECS	EECS	EEPROM, U15	

EECLK	EECLK	EEPROM, U15	
EEDATA	EEDATA	EEPROM, U15	
OSCI	CK12M	12 MHz Oscillator, U16	
DM	D_N	Micro USB 2.0, J10	
DP	D_P	Micro USB 2.0, J10	

FTDI Chip Interfaces and Pins

Serial Configuration Memory

On-board serial configuration memory (U5) is provided by Intel with 16 MBit (2 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration via JTAG interface. The memory is connected to FPGA bank 1 via active serial (AS) x1 interface.

Configuration Memory Pin	Signal Schematic Name	Connected to	Notes
DATA1	AS_DATA0	U1, Bank 1	
DATA0	AS_ASDO	U1, Bank 1	
nCS	AS_nCS	U1, Bank 1	
DCLK	AS_DCLK	U1, Bank 1	

Serial Configuration Memory

Ethernet PHY

The TEI0009 is equipped with two Ethernet PHY (U17, U19) which are connected to two RJ45 (J8, J9) connectors.

Ethernet PHY Pin	Signal Schematic Names (ETH1 /ETH2)	ETH 1	ETH 2	Note
TXD0...3	ETH1_TXD0...3, ETH2_TXD0...3	Bank 5	Bank 5	
TXC	ETH1_TXC, ETH2_TXC	Bank 5	Bank 5	
TXEN	ETH1_TXEN, ETH2_TXEN	Bank 5	Bank 5	
RXD0...3	ETH1_RXD0...3, ETH2_RXD0...3	Bank 5	Bank 5	
RXC/B-CAST_OFF	ETH1_RXC, ETH2_RXC	Bank 5	Bank 5	
RXER/ISO	ETH1_RXER, ETH2_RXER	Bank 5	Bank 5	
INTRP/nNAND_Tree	ETH1_INTRP, ETH2_INTRP	Bank 5	Bank 5	
XI	ETH1_CLKIN, ETH2_CLKIN	Oscillator, U22	Oscillator, U22	
MDC	ETH1_MDC, ETH2_MDC	Bank 5	Bank 5	
MDIO	ETH1_MDIO, ETH2_MDIO	Bank 5	Bank 5	
COL/CONFIG0	ETH1_COL, ETH2_COL	Bank 5	Bank 5	
CRS/CONFIG1	ETH1_CRS, ETH2_CRS	Bank 5	Bank 5	
RXDV/CONFIG2	ETH1_RXDV, ETH2_RXDV	Bank 5	Bank 5	
LED0/NWAYEN	ETH1_LED0, ETH2_LED0	RJ45 - Green LED, J8	RJ45 - Green LED, J9	
LED1/SPEED	ETH1_LED1, ETH2_LED1	RJ45 - Yellow LED, J8	RJ45 - Yellow LED, J9	
nRST	ETH1_RST, ETH2_RST	Bank 5	Bank 5	
RXM	ETH1_RX_N, ETH2_RX_N	RJ45, J8	RJ45, J9	

RXP	ETH1_RX_P, ETH2_RX_P	RJ45, J8	RJ45, J9	
TXM	ETH1_TX_N, ETH2_TX_N	RJ45, J8	RJ45, J9	
TXP	ETH1_TX_P, ETH2_TX_P	RJ45, J8	RJ45, J9	

Ethernet PHY Connections and Pins

EEPROM

TEI0009 has three EEPROM, U15, U18 and U20. U15 is pre-programmed for the FTDI FT2232H configuration. U18 and U19 are used for the MAC address configuration.

Designator	EEPROM Pin	Signal Schematic Names	Connected to	Notes
U15	CS	EECS	FTDI, U14	
	CLK	EECLK	FTDI, U14	
	DIN/DOUT	EEDATA	FTDI, U14	

FTDI and EEPROM Pin Connections

Designator	Pin	Schematic	Connected to	Grove Header	Notes
U18, U20	SCL	I2C_SCL	Bank 6	J5	
	SDA	I2C_SDA	Bank 6	J5	

I2C EEPROM Interface MIOs and Pins

I2C Address	Designator	Notes
0x50	U18	
0x51	U20	

I2C Address for EEPROM

ADC/DAC

The TEI0009 module is equipped with a 12-Bit ADC/DAC (U2).

Pins	Schematic	Connected to	Notes
nRESET	ADDA_RSTN	Bank 2, U1	
nSYNC	ADDA_SYNC	Bank 2, U1	
SCLK	MCLK	Bank 2, U1	
SDI	MOSI	Bank 2, U1	
SDO	MISO	Bank 2, U1	
VREF	AREF	Pin Header, J1	External reference is 1 V to 3.3 V. Internal reference is 2.5 V.
IO0...5	AIN0...5	Bank 1, U1 Pin Header, J4	
IO6	AIN6	Testpoint, TP1	
IO7	AIN7	Testpoint, TP2	

ADC/DAC Interface and Pins

LEDs

Schematic	Designator	Color	Connected to	Active Level	Note
LED1...8	D2...9	Red	Bank 3	High	
LED_PB1...5	D13...17	Red	Bank 7	High	
CONF_DONE	D10	Red	Bank 6	Low	
3.3V	D1	Green	3.3V	High	

On-board LEDs

Push Buttons

Schematic	Designator	Connected to	Functionality	Note
RESET	S7	Bank 1	Reset	
RST_GPIO	S2	Bank 4	Reset/GPIO	
USER_BTN1	S3	Bank 3	User Push Button	
USER_BTN2	S4	Bank 3	User Push Button	
USER_BTN3	S5	Bank 3	User Push Button	
USER_BTN4	S6	Bank 3	User Push Button	
USER_BTN5	S1	Bank 3	User Push Button	

On-board Push Buttons

Clock Sources

Designator	Description	Frequency	Note
U22	Crystal Oscillator	25 MHz	
U16	Crystal Oscillator	12 MHz	

Oscillators

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 3 A for system startup is recommended.

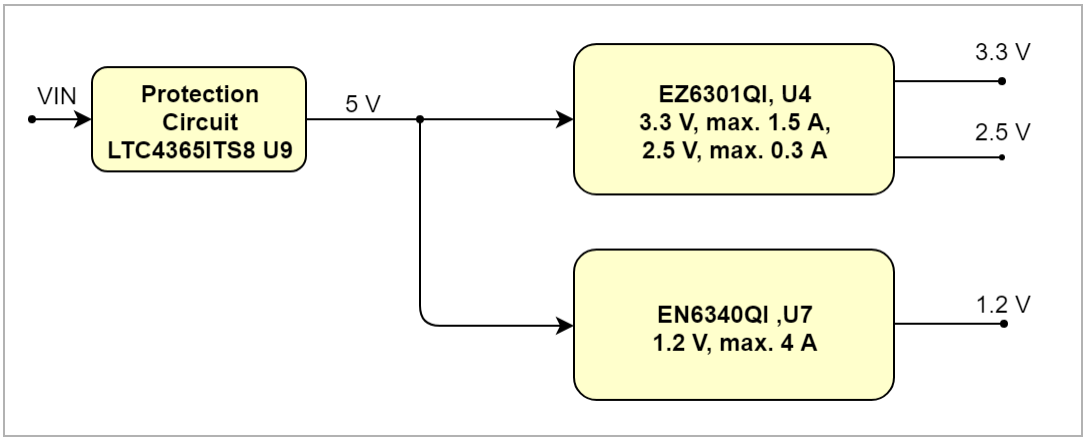
Power Consumption

FPGA	Typical Current
Intel Cyclone 10 LP FPGA	TBD*

Power Consumption

* TBD - To Be Determined

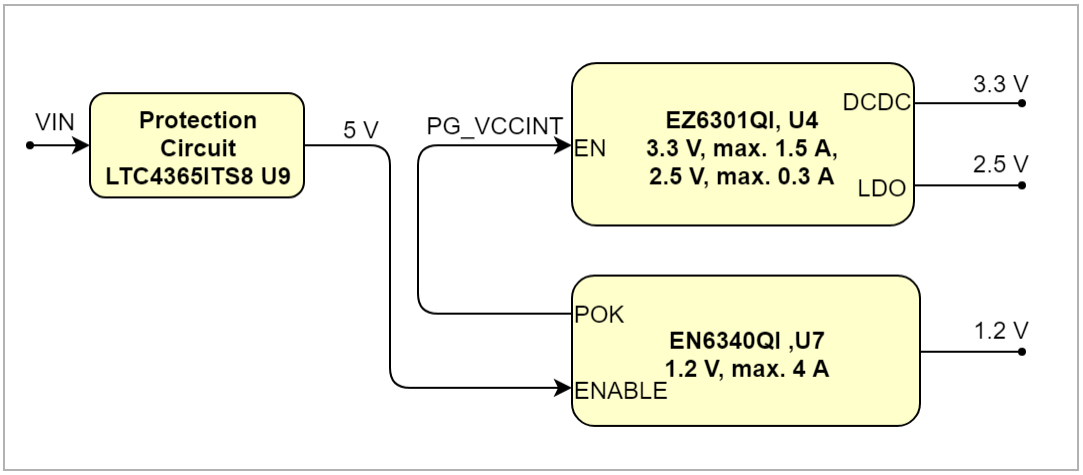
Power Distribution Dependencies



Power Distribution

Power-On Sequence

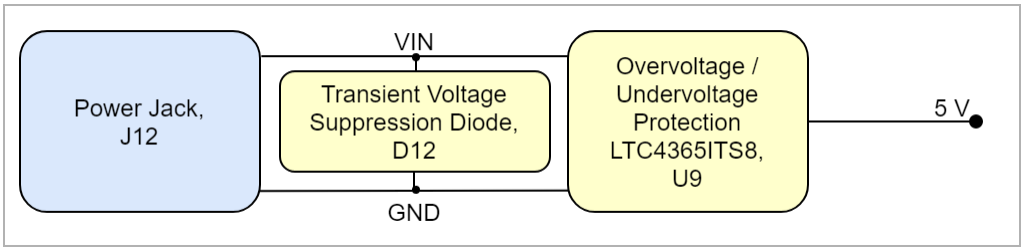
There is the following power-on sequence. The DCDC converter U7 enables the device U4 according to the diagram below.



Power Sequency

Voltage Protection Circuit

There is a transient voltage suppression diode (D12) which protects the board from voltage spikes. Additionaly, there is an overvoltage / undervoltage protection device (U9) for board protection.



Voltage Protection Circuit

Power Rails

Connector Designator	VCCIO Schematic Name	Pin	VCC	Direction	Notes
J12	VIN	1	5 V	In	
J3	3.3V	2, 4	3.3 V	Out	
	5V	5	5 V	Out	
J5	3.3V	3	3.3 V	Out	

Module Power Rails

Bank Voltages

Bank	Schematic Name	Voltage	Notes
Bank 1...8	VCCIO1...8	3.3V	

Intel Cyclone 10 LP Bank Voltages

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit	Note
VIN	Input Supply Voltage (J12)	4.5	5.5	V	
AREF	External Reference Voltage for ADC/DAC (J1 - 8)	-0.3	3.6	V	Only for input usage.
AIN0...5	Input Voltage for ADC/DAC (J4)	-0.3	3.6	V	Only for input usage.
AIN6...7	Input Voltage for ADC/DAC (TP1...2)	-0.3	3.6	V	Only for input usage.
EXT_RST	External Reset (J3 - 3)	-0.5	4.2	V	
D0_RXD, D1_TXD, D2...7	Arduino Interface (J2)	-0.5	4.2	V	Only for input usage.
D8...13, D14_SDA, D15_SCL	Arduino Interface (J1 - 1...6, 9...10)	-0.5	4.2	V	Only for input usage.
I2C_SCL, I2C_SDA	I2C Interface (J5 - 1...2)	-0.3	4.2	V	Only for input usage.
P1_IO1...8, P2_IO1...8, P3_IO1...8, P4_IO1...8, P5_IO1...8, P6_IO1...8,	Pmod Interface (P1...6)	-0.5	4.2	V	Only for input usage.
CLK_IN	External FPGA Clock (J19)	-0.5	4.2	V	
CLK_OUT	Clock / IO (J20)	-0.5	4.2	V	Only for input usage.
T_STG	Storage Temperature	-35	85	°C	See LTC2623WC datasheet

Absolute Maximum Ratings

Recommended Operating Conditions

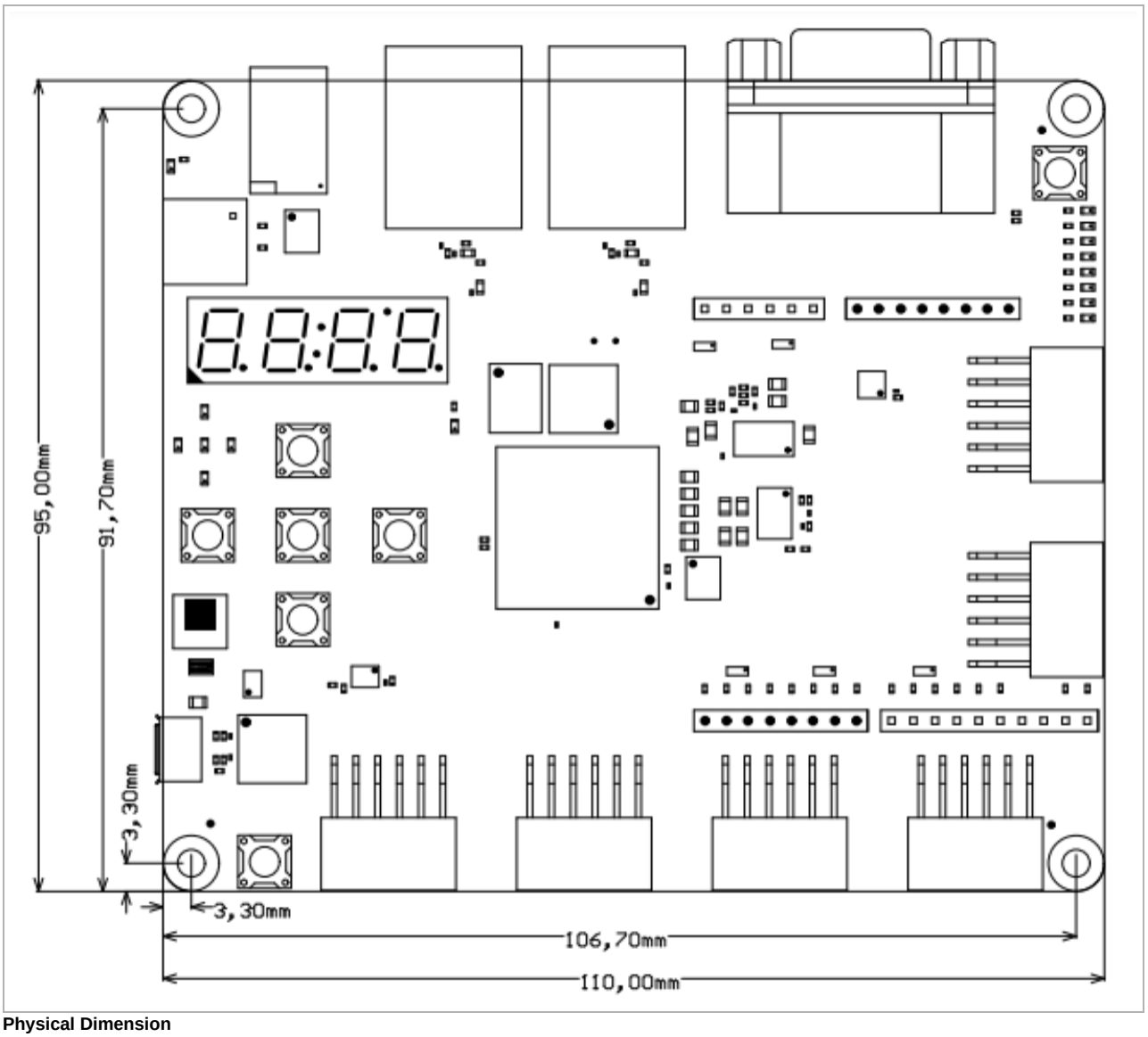
Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Parameter	Min	Max	Units	Reference Document	
VIN	4.75	5.25	V		
AREF	1	3.3	V		
AIN0...5	0	AREF	V		
AIN6...7	0	AREF	V		
EXT_RST	-0.5	3.6	V		
D0_RXD, D1_TXD, D2...7	-0.5	3.6	V		
D8...13, D14_SDA, D15_SCL	-0.5	3.6	V		
I2C_SCL, I2C_SDA	-0.3	3.3	V		
P1_IO1...8, P2_IO1...8, P3_IO1...8, P4_IO1...8, P5_IO1...8, P6_IO1...8,	-0.5	3.6	V		
CLK_IN	-0.5	3.6	V		
CLK_OUT	-0.5	3.6	V		
T_OP	0	70	°C	See SDRAM W9864G6JT datasheet	

Recommended Operating Conditions

Physical Dimensions

- Module size: 95 mm × 110 mm. Please download the assembly diagram for exact numbers.
- PCB thickness: 1.6 mm.



Physical Dimension

Currently Offered Variants

Trenz shop TEI0009 overview page	
English page	German page

Trenz Electronic Shop Overview

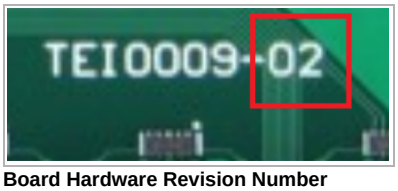
Revision History

Hardware Revision History

Date	Revision	Changes	Document Link
2018-2-19	01	-	---
2018-7-18	02	• Change J5 from SMD Connector to GROVE Connector • Change connection of 12 MHz clock from Bank 1 to Bank 6 • Change connection of I2C SDA/SCL from Bank 3 to Bank 6 • SMA Coaxial Connector J19, J20 not mounted • Change connection of CLK_IN/CLK_OUT from Bank 4 to Bank 8 • Remove DIP Switch S1 • Add 5 LEDs (Red) • Add 2 Push Buttons • Add 64 Mbit QSPI Flash Memory • Change SDRAM Memory • Remove 10-Bit ADC • Remove 10-Bit DAC • Add 12-Bit ADC/DAC • Remove USB Transceiver • Remove 24 MHz Oscillator • Remove DIP Switch S2 • Changed Power Supply Circuit • Add 4 Pmod Host Sockets	REV02

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board Hardware Revision Number

Document Change History

Date	Revision	Contributor	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• initial release

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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