

TE0821 CPLD

Table of contents

- [1 Table of contents](#)
- [2 Overview](#)
 - [2.1 Feature Summary](#)
 - [2.2 Firmware Revision and supported PCB Revision](#)
- [3 Product Specification](#)
 - [3.1 Port Description](#)
 - [3.2 Functional Description](#)
 - [3.2.1 JTAG](#)
 - [3.2.2 Boot Mode](#)
 - [3.2.3 PUDC](#)
 - [3.2.4 Power](#)
 - [3.2.5 LED](#)
- [4 Appx. A: Change History](#)
 - [4.1 Revision Changes](#)
 - [4.2 Document Change History](#)
- [5 Appx. B: Legal Notices](#)
 - [5.1 Data Privacy](#)
 - [5.2 Document Warranty](#)
 - [5.3 Limitation of Liability](#)
 - [5.4 Copyright Notice](#)
 - [5.5 Technology Licenses](#)
 - [5.6 Environmental Protection](#)
 - [5.7 REACH, RoHS and WEEE](#)

Overview

CPLD Device with designator U21: LCMX02-256HC

Feature Summary

- JTAG routing
- Boot Mode settings
- PUDC
- LED

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description
C_TCK	in	30	3.3VIN	JTAG B2B
C_TDI	in	32	3.3VIN	JTAG B2B

C_TDO	out	1	3.3VIN	JTAG B2B
C_TMS	in	29	3.3VIN	JTAG B2B
EN1	in	27	3.3VIN	Power Enable from B2B Connector (Positive Enable) / Used only for PGOOD feedback
User_LED	out	4	3.3VIN	user defined or status, see LED description
N.C.		5	3.3VIN	/ currently_not_used
JTAGEN	in	26	3.3VIN	Enable JTAG access to CPLD for Firmware update (zero: JTAG routed to module, one: CPLD access)
MODE	in	25	3.3VIN	Boot Mode for Zynq/ZynqMP Devices (Flash or SD)
MODE0	out	12	1.8V	ZynqMP Boot Mode Pin 0
MODE1	out	13	1.8V	ZynqMP Boot Mode Pin 1
MODE2	out	14	1.8V	ZynqMP Boot Mode Pin 2
MODE3	out	16	1.8V	ZynqMP Boot Mode Pin 3
NOSEQ	inout	23	3.3VIN	usage CPLD Variant depends
PGOOD	out	28	3.3VIN	Module Power Good (only Feedback from EN1).
PUDC_B	out	17	1.8V	PUD_C external pullup
TCK	out	9	1.8V	JTAG ZynqMP
TDI	out	8	1.8V	JTAG ZynqMP
TDO	in	10	1.8V	JTAG ZynqMP
TMS	out	11	1.8V	JTAG ZynqMP
X0	in	20	VCCO_65	FPGA IO (FPGA Pin B1) / Enable User LED (negative)
X1	in	21	VCCO_65	FPGA IO (FPGA Pin C1)/ Connect to User LED

Functional Description

JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA) on JM1-89.

Boot Mode

Boot Modes can be selected via B2B Pin Mode. Trenz Electronic provides currently 4 Firmware variants, one for SD/JTAG, one for JTAG/QSPI, one for SD /QSPI and SD/QSPI/JTAG usage.

Mode	JTAG/QSPI-Variant	SD/JTAG-Variant	SD/QSPI (default Firmware)	SD/QSPI/JTAG
low	JTAG	Boot from SD	Boot from SD	JTAG Mode, if NOSEQ* is high otherwise boot from SD
high	Boot from Flash	JTAG	Boot from Flash	JTAG Mode, if NOSEQ* is high otherwise boot from Flash

For other UltraScale+ Boot Modes options custom firmware is needed, see also Table 11.1 Boot Modes from Xilinx UG1085.



A special FSBL is provided on 2017.4 or newer reference designs to write boot image to QSPI with Xilinx tools (Vivado or SDK) on Boot Mode unequal JTAG .



NOSEQ*: Please check the carrier board documentation, before using the SD/QSPI/JTAG firmware variant on TE0821. In the most cases special carrier CPLD firmware is needed.

PUDC

const. 1 The I/Os will be 3-stated after power-on when PUDC is High.

Power

PGOOD is EN1. There is no additional power management controlled by CPLD.

LED

LED	Condition
Firmware Variant	if X0 is high (default, if FPGA is not programmed)
User Defined (X1)	if X0 is low

*It's recommended to forward this signal to a carrier LED if status check is needed.

Firmware Variant	Blink sequence	Condition
QSPI/JTAG	*0000000	if boot mode != JTAG otherwise const. high if NOSEQ='1' or const low if NOSEQ='0'
JTAG/SD	**0000000	if boot mode != JTAG otherwise const. high if NOSEQ='1' or const low if NOSEQ='0'
QSPI/SD	****0000 *****000 *****	****0000 if Boot Mod is QSPI otherwise *****000 if NOSEQ='1' or ***** if NOSEQ='0'
SD/QSPI/JTAG	***00000	if boot mode != JTAG otherwise const. high if NOSEQ='1' or const low if NOSEQ='0'

Appx. A: Change History

Revision Changes

- REV00 to REV01
 - copy of TE0820 CPLD Firmware
 - changed PHY_LED1 in to PUDC_B out
 - X0/X1 connected to other FPGA IOs

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV01	REV01		

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]

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Appx. B: Legal Notices

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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REACH, RoHS and WEEE

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Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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