TEI0015 TRM

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Overview

The Trenz Electronic TEI0015 is a commercial-grade, low cost and small size module integrated with Intel® MAX 10. Intel MAX 10 devices are the ideal solution for system management, I/O expansion, communication control planes, industrial, automotive, and consumer applications.

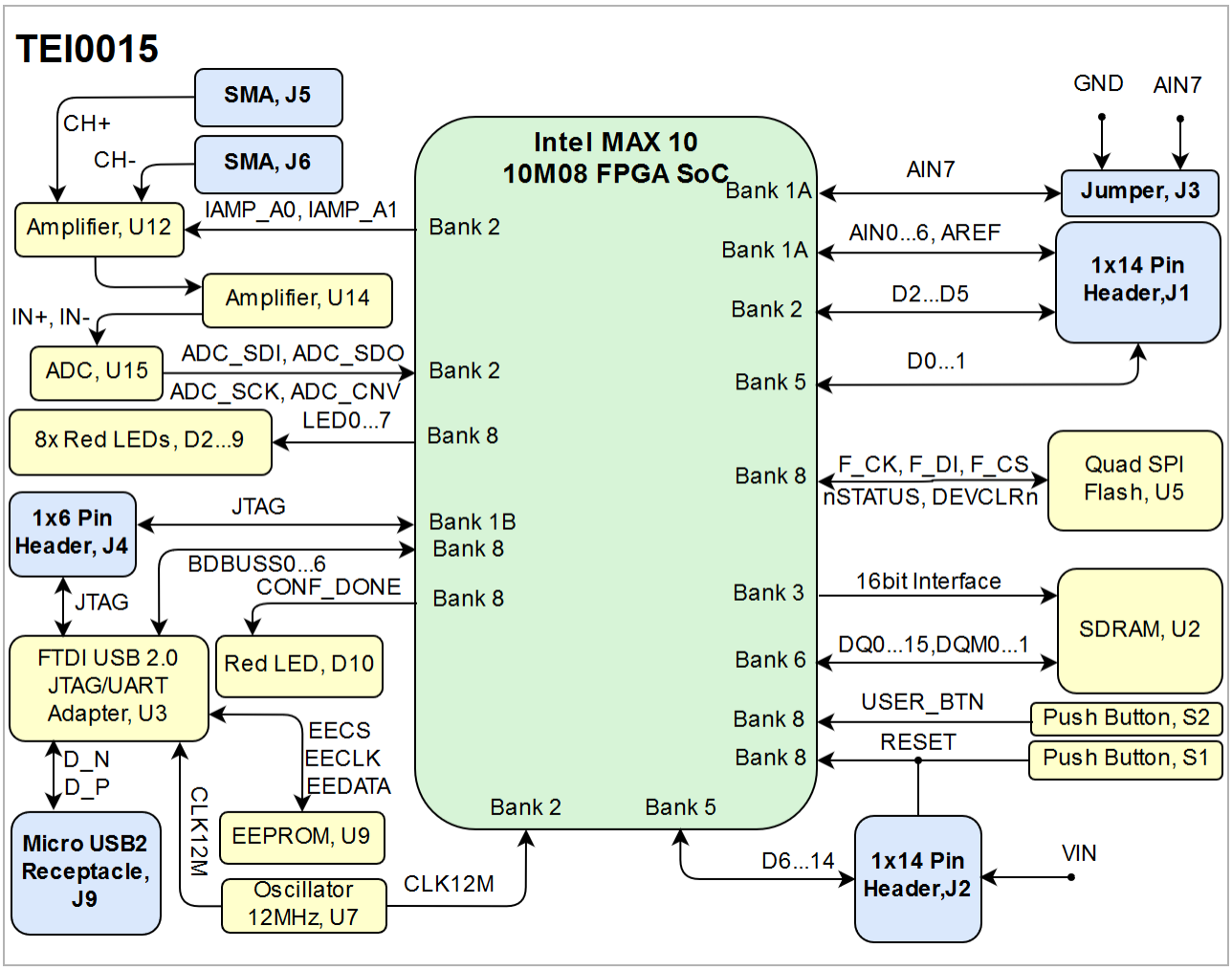
Refer to http://trenz.org/tei0015-info for the current online version of this manual and other available documentation.

Key Features

- Intel® MAX 10 Commercial [10M08SAU169C8G]

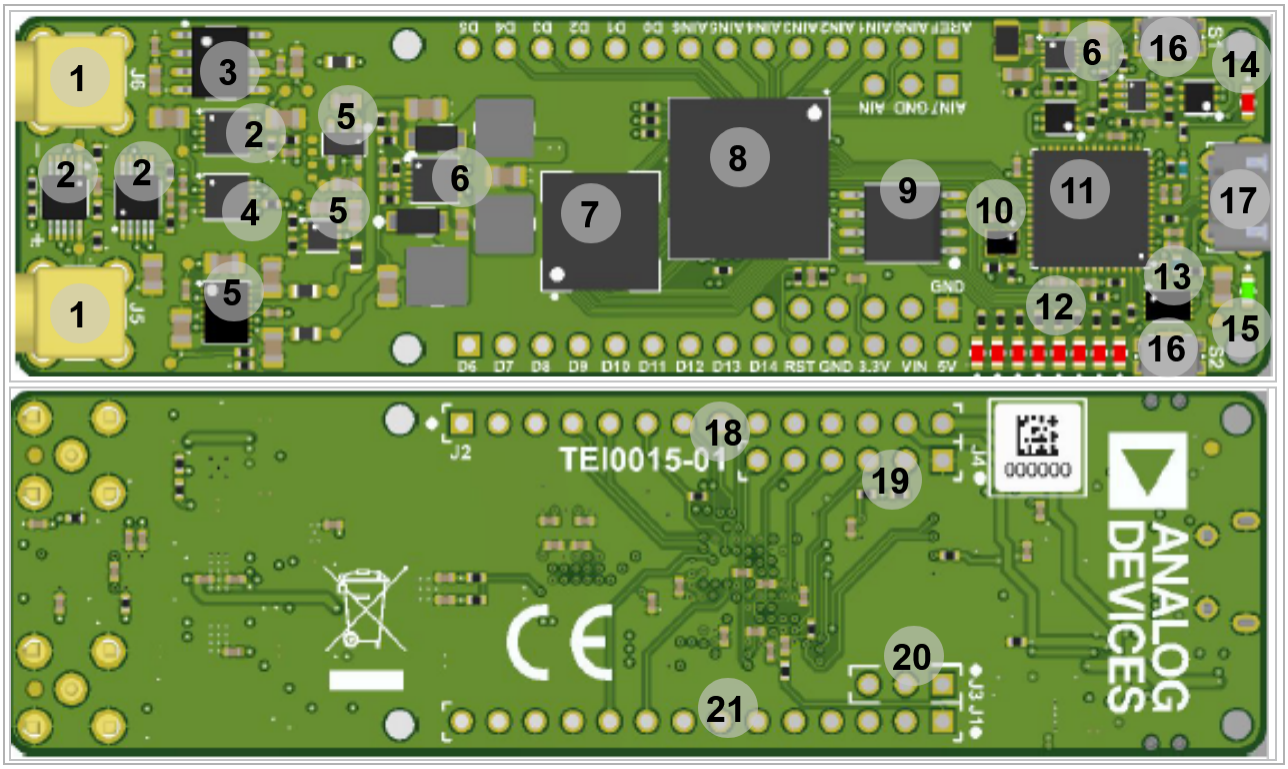
    - Package: UBGA-169
    - Speed Grade: C8 (Slowest)
    - Temperature: 0°C to 85°C
    - Package compatible device 10M08...10M16 as assembly variant on request possible
- SDRAM Memory up to 32 Mbyte (8Mbyte default)
- USB 2.0 Multipurpose UART/FIFO IC (FT2232H)
    - 4 Kbit EEPROM Memory for FTDI configuration data
    - Micro USB Receptacle (communication and power)
- SPI Flash - NOT INSTALLED (only special option)
- 8x User LED
- 18 Bit 2MSPS Analog to Digital Converter
- 2x SMA Female Connector
- I/O interface: 23x GPIO - Arduino MKR compatible
- Power Supply: 5V
- Dimension: 86.5mm x 25mm
- Others:
    - Instrumentation Amplifier
    - Differential Amplifier
    - Operational Amplifier

Block Diagram



TEI0015 block diagram

Main Components



TEI0015 main components

1. SMA Connector, J5...6
2. Amplifier, U12 - U14 - U6
3. Voltage Reference, U8
4. Analog to Digital Converter, U15
5. Voltage Regulator, U10 - U13 - U16
6. Switching Voltage Regulator/LDO, U11 - U4
7. SDRAM Memory, U2
8. Intel® MAX 10 FPGA, U1
9. SPI Flash Memory, U5
10. 12.00 MHz MEMS oscillator, U7
11. FTDI USB2 to JTAG/UART adapter, U3
12. User LEDs, D2...9
13. FTDI configuration EEPROM, U9
14. Configuration/Status LED (Red) , D10
15. Power-on LED (Green), D1
16. Push button, S1...2
17. Micro USB Connector, J9
18. 1x14 pin header, J2 (Not assembled)
19. 1x6 pin header, J4 (Not assembled)
20. 1x4 Header, J3 (Not assembled)
21. 1x14 pin header, J1 (Not assembled)

Initial Delivery State

Storage device name	Content	Notes

Quad SPI Flash	N/A	Not populated
EEPROM	Programmed	FTDI configuration

Initial delivery state of programmable devices on the module

Configuration Signals

The FPGA configuration for Intel MAX 10 FPGAs can be stored through JTAG interface (using a *.POF file) on the FPGA itself since the Intel MAX 10 FPGA offers non-volatile configuration memory on chip. The FPGA configuration is loaded from the non-volatile memory when the board is powered up. To configure the FPGA directly, the JTAG interface can be used to configure the FPGA volatile (using a *.SOF file), means the configuration is lost after power off.

FPGA Reconfigration can be triggered by pressing push button S1.

Signal	Push Button	Pin Header	Note
RESET	S1	J2	Connected to nCONFIG

Reset process.

Signals, Interfaces and Pins

I/Os on Pin Headers and Connectors

FPGA Bank	Connector Designator	I/O Signal Count	Voltage Level	Notes
Bank 1A	J1	7	3.3V	AIN0...6
Bank 1B	J4	5	3.3V	JTAG interface
Bank 2	J1	4	3.3V	DIO2...5
Bank 5	J2	9	3.3V	DIO6...14
	J1	2	3.3V	DIO0...1
Bank 8	J2	1	3.3V	RESET

General I/Os to Pin Headers and connectors information

FPGA I/O Banks

FPGA Bank	I/O Signal Count	Connected to	Notes
Bank 1A	7	1x14 Pin header, J1	AIN0...6
	1	Jumper, J3	AIN7
Bank 1B	5	1x6 Pin header, J4	JTAG_EN, TDI, TDO, TMS, TCK
Bank 2	4	1x14 Pin header, J1	D2...5
	5	A2D, U15	ADC_EN, ADC_SDI, ADC_SDO, ADC_SCK, ADC_CNV
	1	12MHz Oscillator, U7	CLK12M
	2	Amplifier, U12	nIAMP_A0, nIAMP_A1

Bank 3	22	SDRAM, U2	RAM_ADDR_CMD
Bank 5	9	1x14 Pin header, J2	DIO6...14
	2	1x14 Pin header, J1	DIO0...1
	1	D12_R	DIO12
Bank 6	16	SDRAM, U2	DQ0...15
	2	SDRAM, U2	DQM0...1
	1	D11_R	DIO11
Bank 8	8	User Red LEDs, D2...9	LED0...7
	6	SPI Flash, U5	F_CS, F_CKL, F_DI, F_DO, nSTATUS, DEVCLRn
	1	Red LED, D10	CONF_DONE
	6	FTDI JTAG/UART Adapter, U3	BDBUS0...5
	1	Push Button, S2	USER_BTN

FPGA I/O Banks

Micro-USB Connector

The Micro-USB connector J9 provides an interface to access the FIFO/UART and JTAG functions via FTDI FT2232 chip. The use of this feature requires that FTDI USB drivers are installed on your host PC.

Pins	Connected to	Note
VBUS	USB_VBUS	
D+	FTDI FT2232H U3, DP pin	
D-	FTDI FT2232H U3, DM pin	

Micro USB-2 connector pins

JTAG Interface

JTAG access to the TEI0015 SoM through pin header connector J4. This is normally not needed as there is on-board USB JTAG functionality.

JTAG Signal	Pin Header Connector	Note
TMS	J4-6	
TDI	J4-5	
TDO	J4-4	
TCK	J4-3	
JTAG_EN	J4-2	Pulled-up to 3.3V

JTAG pins connection

On-board Peripherals

Chip/Interface	Designator	Notes

TEI0015 TRM#SDRAM	U2	
FTDI FT2232H	U3	JTAG/UART/FIFO
SPI Flash	U5	
TEI0015 TRM#EEPROM	U9	
Oscillator	U7	12 MHz clock source
TEI0015 TRM#ADC	U12, U14	Analog to Digital Converter
Push Buttons	S1...2	
8x User LEDs	D2...9	Red LEDs

On board peripherals

SDRAM

TEI0015 is equipped with a Winbond 64 MBit (8 MByte) SDRAM chip in standard configuration, variants with 256 Mbit (32 MByte) memory density are also available. The SDRAM chip is connected to the FPGA bank 3 and 6 via 16-bit memory interface with 166MHz clock frequency and CL3 CAS latency.

SDRAM I/O Signals	Signal Schematic Name	Connected to	Notes
Address inputs	A0 ... A13	bank 3	-
Bank address inputs	BA0 / BA1	bank 3	-
Data input/output	DQ0 ... DQ15	bank 6	-
Data mask	DQM0 ... DQM1	bank 6	-
Clock	CLK	bank 3	-
Control Signals	CS	bank 3	Chip select
	CKE	bank 3	Clock enable
	RAS	bank 3	Row Address Strobe
	CAS	bank 3	Column Address Strobe
	WE	bank 3	Write Enable

SDRAM interface IOs and pins

FTDI FT2232H

The FTDI chip U3 converts signals from USB2 to a variety of standard serial and parallel interfaces. Refer to the FTDI data sheet to get information about the features of the FT2232H chip. FTDI FT2232H chip channel A is used in MPPSE mode for JTAG. Channel B is configured to be used in async FIFO mode, this is default mode when using preprogrammed FTDI configuration. In this mode the communication from host PC looks like normal UART but from the FTDI side it is 8 bit FIFO style interface.

The configuration of FTDI FT2232H chip is pre-programmed in the EEPROM U9.

FTDI Chip U3 Pin	Signal Schematic Name	Connected to	Notes
ADBUS0	TCK	FPGA bank 1B, pin G2	JTAG interface
ADBUS1	TDI	FPGA bank 1B, pin F5	
ADBUS2	TDO	FPGA bank 1B, pin F6	

ADBUS3	TMS	FPGA bank 1B, pin G1	
BDBUS0	BDBUS0	FPGA bank 8, pin A4	User configurable
BDBUS1	BDBUS1	FPGA bank 8, pin B4	User configurable
BDBUS2	BDBUS2	FPGA bank 8, pin B5	User configurable
BDBUS3	BDBUS3	FPGA bank 8, pin A6	User configurable
BDBUS4	BDBUS4	FPGA bank 8, pin B6	User configurable
BDBUS5	BDBUS5	FPGA bank 8, pin A7	User configurable
BDBUS6	BDBUS6	FPGA bank 6, pin C11	
BDBUS7	BDBUS7	FPGA bank 3, pin J7	
BCBUS0	BCBUS0	FPGA bank 5, pin J9	
BCBUS1	BCBUS1	FPGA bank 3, pin K5	
BCBUS2	BCBUS2	FPGA bank 3, pin L4	
BCBUS3	BCBUS3	FPGA bank 3, pin L5	
BCBUS4	BCBUS4	FPGA bank 3, pin N12	

FTDI chip interfaces and pins

SPI Flash

Optional SPI flash device maybe assembled in custom variants, normally it is not populated.

Signal Schematic Name	Connected to	Notes
F_CS	FPGA bank 8, pin B3	Chip select
F_CLK	FPGA bank 8, pin A3	Clock
F_DI	FPGA bank 8, pin A2	Data in / out
nSTATUS	FPGA bank 8, pin C4	Data in / out, configuration dual-purpose pin of FPGA
DEVCLRN	FPGA bank 8, pin B9	Data in / out, configuration dual-purpose pin of FPGA
F_DO	FPGA bank 8, pin B2	Data in / out

Quad SPI Flash memory interface

EEPROM

The configuration of FTDI FT2232H chip is pre-programmed in the EEPROM U9.

Schematic	Connected to	Notes
EECS	FTDI U3, Pin EECS	
EECLK	FTDI U3, Pin EECLK	
EEDATA	FTDI U3, Pin EEDATA	

I2C EEPROM interface MIOs and pins

ADC

The TEI0015 board is equipped with the Analog Devices AD4003BCPZ-RL7 18-bit 2MSPS ADC.

Pins	Connected to	Notes
IN+	Diff Amplifier U14, VOUT-	
IN-	Diff Amplifier U14, VOUT+	
SDI	FPGA, bank 2, pin M2, ADC_SDI	
SDO	FPGA, bank 2, pin M1, ADC_SDO	
SCK	FPGA, bank 2, pin N3, ADC_SCK	
CNV	FPGA, bank 2, pin N2, ADC_CNV	

A2D converter interface and pins

LEDs

Designator	Color	Connected to	Active Level	Note
D2...9	Red	LED1...8	Active High	User LEDs
D10	Red	CONF_DONE	Active Low	Configuration DONE LED
D1	Green	3.3V	Active High	After power on it will be on.

On-board LEDs

Push Bottuns

Designator	Connected to	Functionality	Note
S1	RESET	General reset	
S2	USER_BTN	User push button	Connected to FPGA Bank 8.

On-board Push Buttons

Clock Sources

Clock Source	Schematic Name	Frequency	Note
MEMS Oscillator, U7	CLK12M	12.00 MHz	Connected to FTDI FT2232 U3, pin 3. Connected to FPGA SoC bank 2, pin H6.

Osillators

Power and Power-On Sequence

Power Supply

The module is power supplied from USB (optionally via unpopulated pin header).

Power Consumption

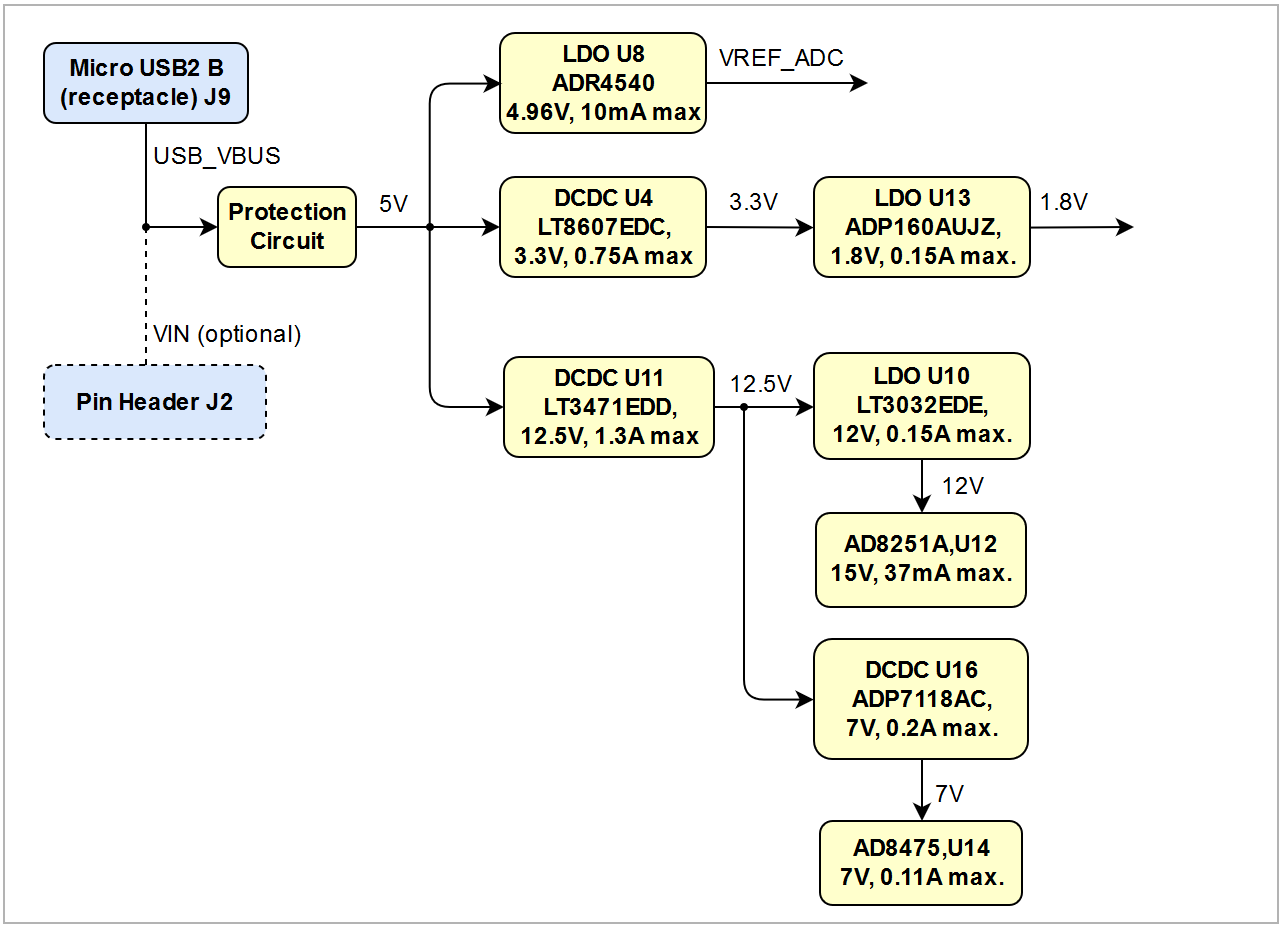
FPGA	Typical Current
Intel MAX 10 10M08 FPGA	TBD*

Power Consumption

* TBD - To Be Determined

Actual power consumption depends on the FPGA design and ambient temperature.

Power Distribution Dependencies



Power Distribution

Power-On Sequence

There is no specific or special power-on sequence, just one single power source is needed. After power on the green LED (D1) will be on.

Power Rails

Power Rail Name	Connector J2 Pin	Connector J9 Pin	Direction	Notes
VIN	J2-13	-	Input	5 V - Pin Header
3.3V	J2-12	-	Output	
5V	J2-14	-	Output	
USB_VBUS	-	J9-1	Input	5 V - USB Connector

Module power rails.

Bank Voltages

Bank	Schematic Name	Voltage	Notes
Bank 1A	VCCIO1A	3.3V	
Bank 1B	VCCIO1B	3.3V	
Bank 2	VCCIO2	3.3V	
Bank 3	VCCIO3	3.3V	
Bank 5	VCCIO5	3.3V	
Bank 6	VCCIO6	3.3V	
Bank 8	VCCIO8	3.3V	

Intel MAX 10 SoC bank voltages.

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit	Reference Document
VIN	Supply voltage	4.75	5.25	V	
CH1-, CH1+	Analog input voltage on amplifier U12 pin 1, 10	-30	30	V	AD8251 datasheet
T_STG	Storage Temperature	-25	+85	°C	

Absolute maximum ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

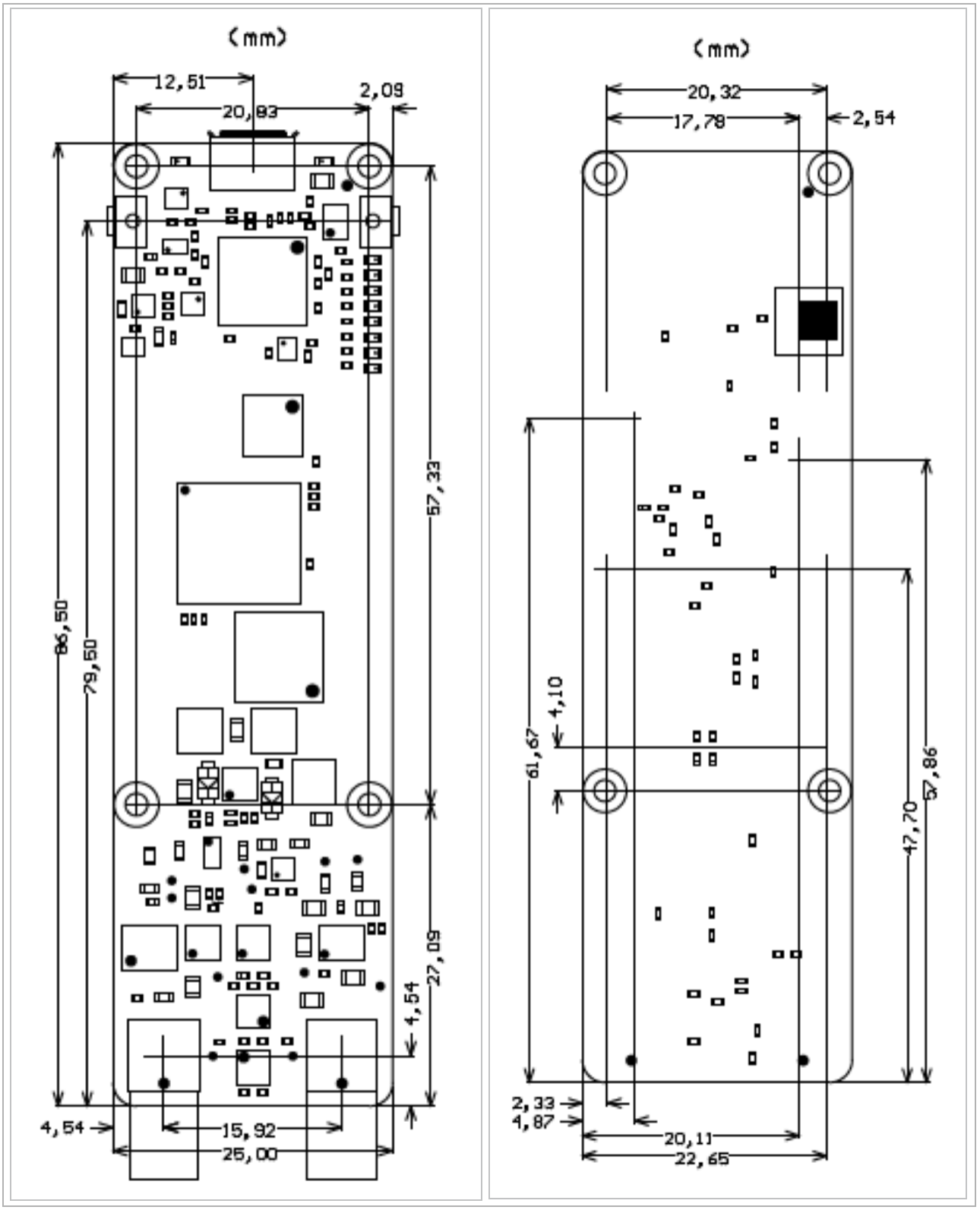
Symbols	Min	Max	Unit	Reference Document
VIN supply voltage (5.0V nominal)	4.75	5.25	V	
Analog input voltage on amplifier U12 pin 1 (CH1-), 10 (CH1+)	-10	10	V	AD8251 datasheet
T_OP	0	+70	°C	W9864G6JT-6 datasheet

Recommended operating conditions.

Physical Dimensions

Module size: 25 mm × 86.5 mm. Please download the assembly diagram for exact numbers.

PCB thickness: 1.22 mm.


(mm)
12,51
20,83
2,09
57,33
86,50
79,50
27,09
4,54
4,54
15,92
25,00
(mm)
20,32
17,78
2,54
4,10
61,67
57,86
47,70
2,33
4,87
20,11
22,65

Physical Dimension

Currently Offered Variants

Trenz shop TEI0015 overview page	
English page	German page

Trenz Electronic Shop Overview

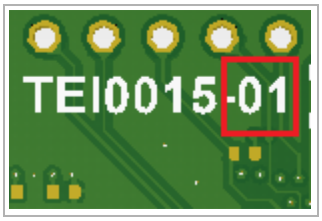
Revision History

Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-02-11	01	-	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board hardware revision number.

Document Change History

Date	Revision	Contributor	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• multiple sections updated
2020-02-04	v.98	ED	• Technical Specifications updated • Power Rails updated

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Document change history.

Disclaimer

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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