

# TEI0006 TRM

[Download PDF version of this document.](#)

## Table of Contents

- [Overview](#)
  - [Key Features](#)
  - [Block Diagram](#)
  - [Main Components](#)
  - [Initial Delivery State](#)
  - [Configuration Signals](#)
- [Signals, Interfaces and Pins](#)
  - [Board to Board \(B2B\) I/Os](#)
  - [JTAG Interface](#)
  - [MIO Pins](#)
- [On-board Peripherals](#)
  - [QSPI Flash Memory](#)
  - [EEPROM](#)
  - [DDR3 SDRAM](#)
  - [Ethernet PHY](#)
  - [Intel MAX 10](#)
  - [LEDs](#)
  - [Clock Sources](#)
  - [CryptoAuthentication](#)
- [Power and Power-On Sequence](#)
  - [Power Supply](#)
  - [Power Consumption](#)
  - [Power Distribution Dependencies](#)
  - [Power-On Sequence](#)
  - [Power Rails](#)
  - [Bank Voltages](#)
- [Board to Board Connectors](#)
  - [Connector Speed Ratings](#)
  - [Current Rating](#)
  - [Connector Mechanical Ratings](#)
  - [Manufacturer Documentation](#)
- [Technical Specifications](#)
  - [Absolute Maximum Ratings](#)
  - [Recommended Operating Conditions](#)
  - [Physical Dimensions](#)
- [Currently Offered Variants](#)
- [Revision History](#)
  - [Hardware Revision History](#)
  - [Document Change History](#)
- [Disclaimer](#)
  - [Data Privacy](#)
  - [Document Warranty](#)
  - [Limitation of Liability](#)
  - [Copyright Notice](#)
  - [Technology Licenses](#)
  - [Environmental Protection](#)
  - [REACH, RoHS and WEEE](#)

## Overview

The Trenz Electronic TEI0006 is an industrial grade module based on Intel® Cyclone 10 GX. Intel® Cyclone 10 GX device family delivers higher core, transceiver, and I/O performance than the previous generation of low cost FPGAs.

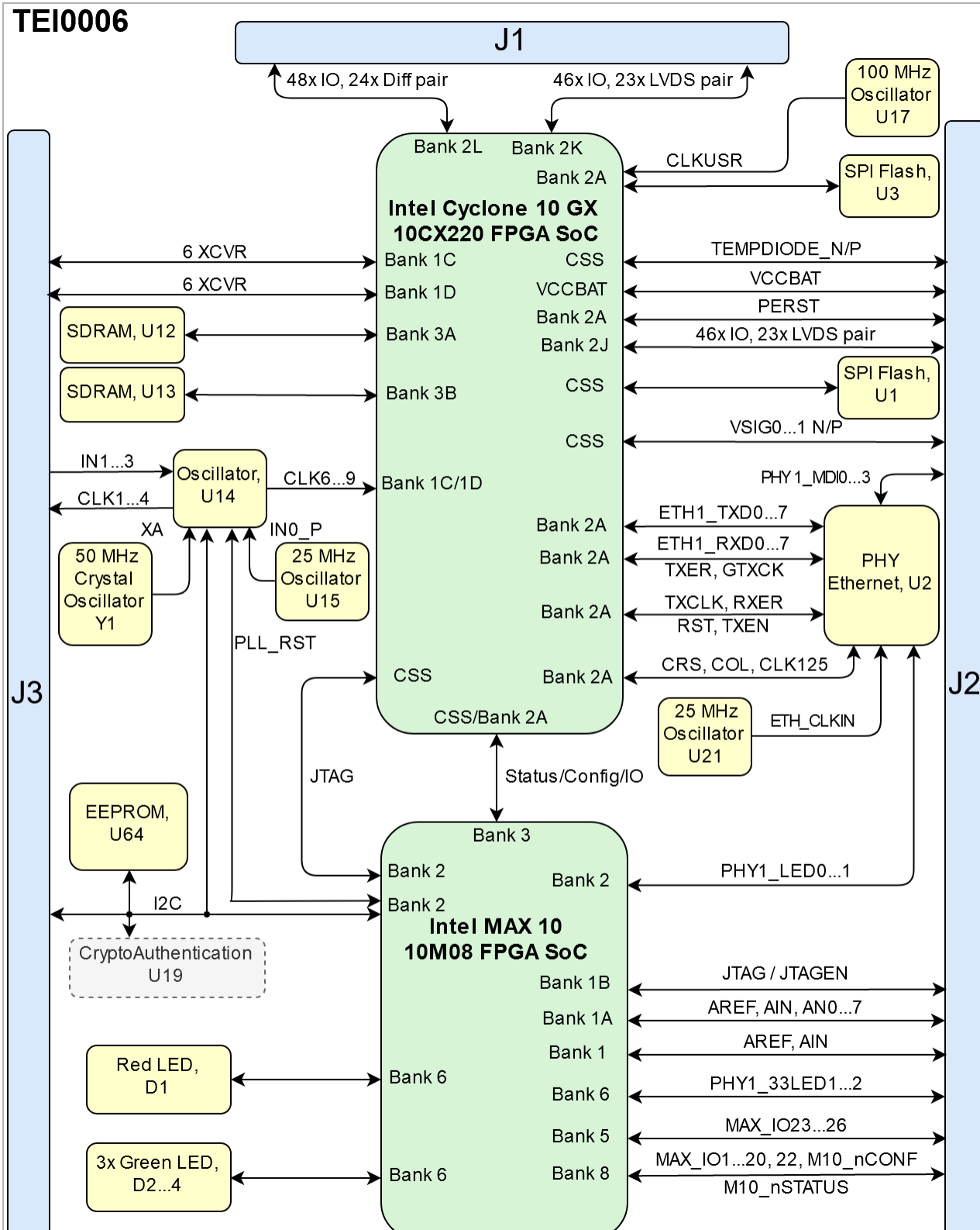
Refer to <http://trenz.org/tei0006-info> for the current online version of this manual and other available documentation.

## Key Features

- Intel® Cyclone 10 GX Industrial [10CX220YF780I5G]
  - Package: FBGA-780
  - Speed Grade: 5 (Fastest)
  - Temperature: -40°C to 100°C
  - Package compatible device 10CX150 and 10CX105 as assembly variant on request possible
- 2x SDRAM DDR3L Memory IC 8 Gbit (1 GByte), Half rate: 533 MHz; Quarter rate: max. 800 MHz
- 2x SPI Flash, 1 Gbit (128 MByte)
- 1x Gigabit Ethernet
- 10-Channel, Any-Frequency, Any-Output Jitter Attenuator/Clock Multiplier
- Intel® MAX 10 as System Controller (CPLD)
- 2 Kbit EEPROM Memory
- 4x User LED
- I/O interfaces: 226/94/46 (IOs/DIFF. Pairs/LVDS Pairs)
- 12 x 12.5Gbps Transceiver
- Board to Board (B2B) Connection: Plug-on module with 3 x 160-pin Samtec Razor Beam (ST5) connectors
- 5 V Power Supply
- Dimension: 80m x 60m

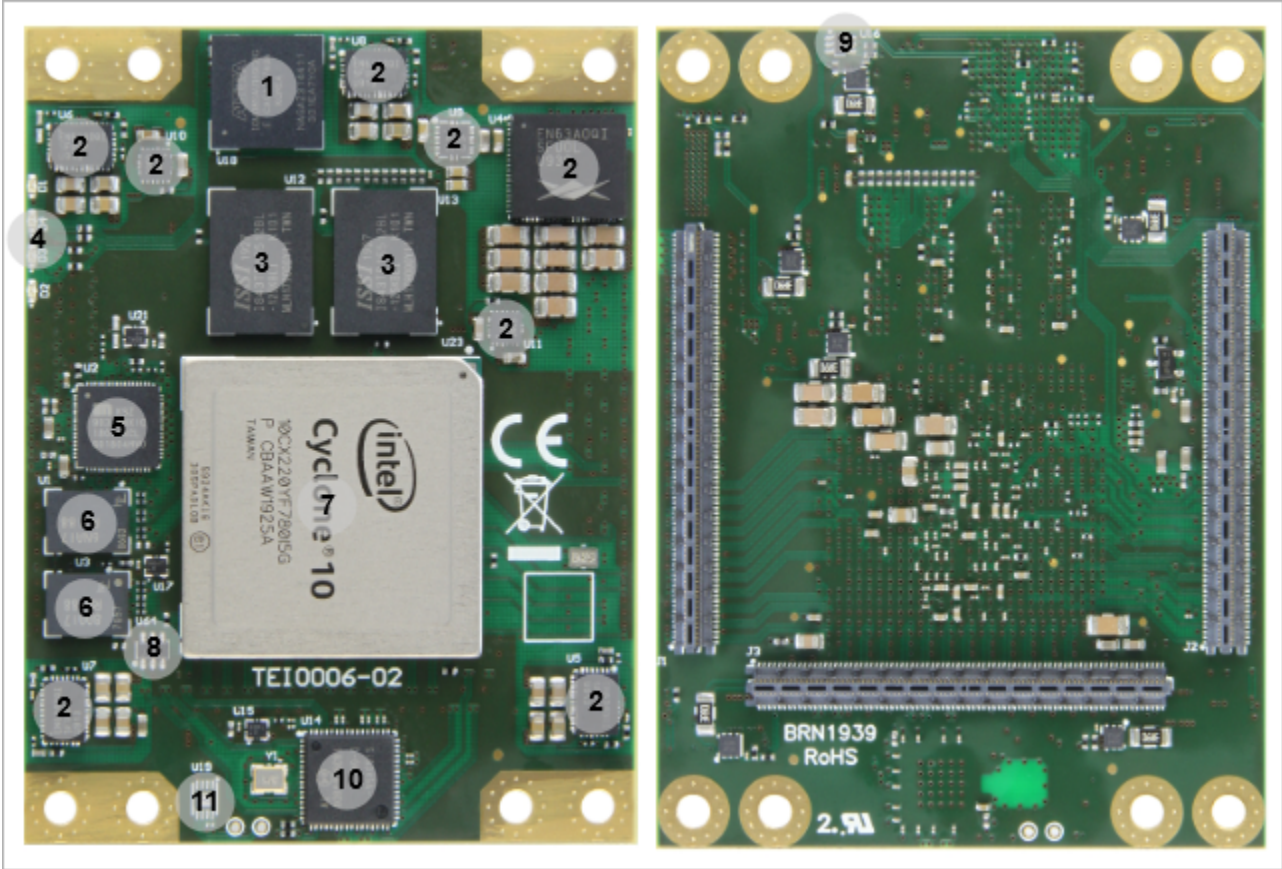
## Block Diagram

## J3



TEI0006 block diagram

Main Components



TEI0006 main components

- 1. Intel® MAX 10, U18
- 2. DC/DC convertor, U4...11
- 3. SDRAM DDR3 Memory, U12 - U13
- 4. User LEDs, D1...4
- 5. Ethernet Transceiver, U2
- 6. SPI Flash Memory, U1 - U3
- 7. Intel® Cyclone 10 GX, U23
- 8. EEPROM, U64
- 9. Buffer, U16
- 10. 10-Channel Clock Multiplier, U14
- 11. CryptoAuthentication Device (optional), U19

Initial Delivery State

| Storage device name | Content    | Notes             |
|---------------------|------------|-------------------|
| Intel® MAX 10       | Programmed | See CPLD Firmware |

|                |                |              |
|----------------|----------------|--------------|
| Quad SPI Flash | Not Programmed |              |
| EEPROM         | Programmed     | Ethernet MAC |
| DDR3 SDRAM     | Not Programmed |              |

**Initial delivery state of programmable devices on the module**

## Configuration Signals

The TEI0006 module can be configured using different modes. Mode selection can be done using MSEL[2:0]. MSEL2 is connected to GND so mode selection can be done using MSEL[1:0] which are connected to Bank 3 of Intel Max 10.

| MODE Signal State | MSEL2 | MSEL1 | MSEL0 | Boot Mode             |
|-------------------|-------|-------|-------|-----------------------|
| MSEL[2:0]         | 0     | 1     | 0     | AS / Fast             |
|                   | 0     | 1     | 1     | AS / Standard         |
|                   | 0     | 0     | 0     | PS and FPP / Fast     |
|                   | 0     | 0     | 1     | PS and FPP / Standard |

**Boot process.**

By tying the CONF\_DONE, NSTATUS, and NCONFIG pins together, the devices initialize and enter user mode at the same time. If any device in the chain detects an error, configuration stops for the entire chain and you must reconfigure all the devices. For example, if the first device in the chain flags an error on the NSTATUS pin, it resets the chain by pulling its NSTATUS pin low.

| Signals      | Connected to | Description           | Note                                                     |
|--------------|--------------|-----------------------|----------------------------------------------------------|
| NCONFIG      | 1.8V         | Configuration trigger | From U18 (Intel MAX 10) - Bank 3                         |
| CONF_DONE    | 1.8V         | Configuration done    | To U18 (Intel MAX 10) - Bank 3                           |
| NSTATUS      | 1.8V         | Configuration status  | To U18 (Intel MAX 10) - Bank 3                           |
| DCLK         | U1           | Configuration clock   | To U1 (Flash Memory)<br>From U18 (Intel MAX 10) - Bank 3 |
| AS_DATA0...3 | U1           | Configuration data    | From U1 (Flash Memory)                                   |

**Configuration signals.**

| Signal | B2B   | Connected to | Note |
|--------|-------|--------------|------|
| PERST  | J2-99 | Bank A2      |      |

**Reset process.**

## Signals, Interfaces and Pins

### Board to Board (B2B) I/Os

FPGA bank number and number of I/O signals connected to the B2B connector:

| FPGA                | FPGA Bank | B2B Connector | I/O Signal Count | Voltage Level | Notes                                  |
|---------------------|-----------|---------------|------------------|---------------|----------------------------------------|
| Intel Cyclone 10 GX | Bank 1C   | J3            | 12 Diff pair     | 0.95V         | GXBL1C_RX0...5 N/P, GXBL1C_TX0...5 N/P |
|                     | Bank 1D   | J3            | 12 Diff pair     | 0.95V         | GXBL1D_RX0...5 N/P, GXBL1D_TX0...5 N/P |

|              |         |    |                                |                |               |
|--------------|---------|----|--------------------------------|----------------|---------------|
|              | Bank 2A | J2 | 2 Single ended                 | 1.8V           | PERST, CLKUSR |
|              | Bank 2J | J2 | 46 Single ended (23 Diff pair) | VCCIO2J        |               |
|              | Bank 2K | J1 | 46 Single ended (23 Diff pair) | VCCIO2K        |               |
|              | Bank 2L | J1 | 48 Single ended (24 Diff pair) | VADJ up to 3 V |               |
|              | Bank 3A | -  | -                              | 1.35V          | VDD_DDR       |
|              | Bank 3B | -  | -                              | 1.35V          | VDD_DDR       |
| Intel Max 10 | Bank 1A | J2 | 8 Single ended                 | 3.3V           |               |
|              | Bank 1B | J2 | 5 Single ended                 | 3.3V           |               |
|              | Bank 2  | J3 | 1 Single ended                 | 1.8VIO         |               |
|              | Bank 3  | -  | -                              | 1.8VIO         |               |
|              | Bank 5  | J2 | 3 Single ended                 | 3.3V           |               |
|              | Bank 6  | J2 | 2 Single ended                 | 3.3V           |               |
|              | Bank 8  | J2 | 23 Single ended                | 3.3V           |               |

**General PL I/O to B2B connectors information**

## JTAG Interface

JTAG access to the TEI0006 SoM is through B2B connector J2. JTAGEN is pulled up to 3.3V and after power on, JTAG for MAX 10 CPLD is enabled. JTAG port of Cyclon 10 GX device is routed to MAX10 CPLD IOs. The default Firmware connects the JTAG port of the Cyclon 10 GX to the IO pins of the JTAG port in user IO mode. Setting JTAGEN to GND enables JTAG for the Cyclon 10 GX device.

| JTAG Signal | B2B Connector | Note               |
|-------------|---------------|--------------------|
| TMS         | J2-160        |                    |
| TDI         | J2-159        |                    |
| TDO         | J2-158        |                    |
| TCK         | J2-157        |                    |
| JTAGEN      | J2-105        | Pulled up to 3.3V. |

**JTAG pins connection**

## MIO Pins

| MIO Pin          | Connected to                | B2B | Notes |
|------------------|-----------------------------|-----|-------|
| MAX_IO1...20, 22 | U18 (Intel MAX 10) - Bank 8 | J2  |       |
| MAX_IO23, 25, 26 | U18 (Intel MAX 10) - Bank 5 | J2  |       |

**MIOs pins**

## On-board Peripherals

| Chip/Interface              | Designator             | Notes                    |
|-----------------------------|------------------------|--------------------------|
| QSPI Flash Memory           | U1 - U3                | U1- AS configuration     |
| EEPROM                      | U64                    |                          |
| DDR3 SDRAM Memory           | U12 - U13              |                          |
| Ethernet PHY                | U2                     |                          |
| Intel Max 10                | U18                    | System controller        |
| User LEDs                   | D1...4                 | D1 (Red), D2...4 (Green) |
| Oscillators                 | U14, U15, U17, U21, Y1 |                          |
| CryptoAuthentication Device | U19                    | optional                 |

#### On board peripherals

## QSPI Flash Memory

The TEI0006 is equipped with two Micron SPI flash memory. On-board SPI flash memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency.

| Designator | Schematic  | Connected to                  | Notes                                      |
|------------|------------|-------------------------------|--------------------------------------------|
| U1         | NCSO       | CSS Bank (Configuration Bank) | Used when you are not configuring using AS |
|            | DCK        | DCLK                          | AS Configuration Clock                     |
|            | AS_DATA0   | CSS Bank (Configuration Bank) |                                            |
|            | AS_DATA1   | CSS Bank (Configuration Bank) |                                            |
|            | AS_DATA2   | CSS Bank (Configuration Bank) |                                            |
|            | AS_DATA3   | CSS Bank (Configuration Bank) |                                            |
| U3         | QSPI_CS    | Bank 2A                       |                                            |
|            | QSPI_CK    | Bank 2A                       |                                            |
|            | QSPI_DATA0 | Bank 2A                       |                                            |
|            | QSPI_DATA1 | Bank 2A                       |                                            |
|            | QSPI_DATA2 | Bank 2A                       |                                            |
|            | QSPI_DATA3 | Bank 2A                       |                                            |

#### Quad SPI interface MIOs and pins

## EEPROM

| Schematic | U64 EEPROM Pin | B2B    | U18 Intel Max 10 Pin | Notes |
|-----------|----------------|--------|----------------------|-------|
| I2C_SCL   | SCL            | J3-135 | Bank 2 - K2          |       |
| I2C_SDA   | SDA            | J3-137 | Bank 2 - L2          |       |

#### I2C EEPROM interface MIOs and pins

| Pins             | I2C Address | Designator | Notes |
|------------------|-------------|------------|-------|
| I2C_SCL, I2C_SDA | 0x53        | U64        |       |

**I2C address for EEPROM**

**DDR3 SDRAM**

The TEI0006 SoM has two 1 GByte volatile DDR3 SDRAM IC provided by Integrated Silicon Solution Inc for storing user application code and data.

- Part number: IS43TR16512BL
- Supply voltage: 1.35 V
- Speed: Half rate: 533 MHz; Quarter rate: max. 800 MHz
- Temperature: -40 °C to 95 °C

**Ethernet PHY**

| Signal Name   | Connected to | B2B   | Signal Description           |
|---------------|--------------|-------|------------------------------|
| PHY1_MDI0_P   | -            | J2-93 |                              |
| PHY1_MDI0_N   | -            | J2-91 |                              |
| PHY1_MDI1_P   | -            | J2-87 |                              |
| PHY1_MDI1_N   | -            | J2-85 |                              |
| PHY1_MDI2_P   | -            | J2-81 |                              |
| PHY1_MDI2_N   | -            | J2-79 |                              |
| PHY1_MDI3_P   | -            | J2-75 |                              |
| PHY1_MDI3_N   | -            | J2-73 |                              |
| ETH1_RST      | U23, Bank 2A | -     | Pulled-up to DVDDH Voltage.  |
| ETH1_MDC      | U23, Bank 2A | -     | Pulled-up to DVDDH Voltage.  |
| ETH1_MDIO     | U23, Bank 2A | -     | Pulled-up to DVDDH Voltage.  |
| ETH1_TXD0...7 | U23, Bank 2A | -     | 8 bit Transfer               |
| ETH1_RXD0...7 | U23, Bank 2A | -     | 8 bit Receive                |
| ETH1_GTXCK    | U23, Bank 2A | -     |                              |
| ETH1_TXCLK    | U23, Bank 2A | -     |                              |
| ETH1_TXEN     | U23, Bank 2A | -     |                              |
| ETH1_TXER     | U23, Bank 2A | -     |                              |
| ETH1_RXCK     | U23, Bank 2A | -     | Pulled-down to GND.          |
| ETH1_RXDV     | U23, Bank 2A | -     | Pulled-down to GND.          |
| PHY1_INT      | -            | -     | Pulled-up to DVDDH Voltage.  |
| PHY1_LED1     | U18, Bank 2  | -     | Pulled-up to DVDDH Voltage.  |
| PHY1_LED2     | U18, Bank 2  | -     | Pulled-down to GND.          |
| ETH1_CRS      | U23, Bank 2A | -     |                              |
| ETH1_XTAL_IN  | ETH_CLKIN    | -     | From U21 (25 MHz Oscillator) |

**Ethernet PHY to Intel Cyclone 10 GX SoC connections**

**Intel MAX 10**

The TEI0006 is equipped with an Intel MAX 10 device which is a single-chip, non-volatile low-cost programmable logic device (PLD) to integrate the optimal set of system components. Intel MAX 10 (U18) is power and configuration controller on TEI0006 SoM.

| Intel Max 10 Bank | Signals                     | Connected to                                           | Description                                               | Notes               |
|-------------------|-----------------------------|--------------------------------------------------------|-----------------------------------------------------------|---------------------|
| Bank 1A           | AIN0...7                    | B2B- J2                                                |                                                           |                     |
| Bank 1B           | TCK, TDO, TMS, TDI, JTAGEN  | B2B- J2                                                |                                                           |                     |
| Bank 2            | PHY1_LED1                   | Ethernet PHY, U2                                       | Ethernet LED                                              | Pulled-up to DVDDH. |
|                   | PHY1_LED2                   | Ethernet PHY, U2                                       | Ethernet LED                                              | Pulled-down to GND. |
|                   | F_TCK, F_TDO, F_TDI, F_TMS  | Intel Cyclone 10 GX (U23) - Bank CSS                   | Intel Cyclone 10 JTAG signals                             |                     |
|                   | I2C_SDA, I2C_SCL            | EEPROM, U64<br>B2B, J3<br>Programmable Oscillator, U14 | I2C EEPROM signals                                        |                     |
|                   | PLL_RST                     | Programmable Oscillator, U14                           | Oscillator reset signal                                   |                     |
| Bank 3            | NSTATUS, NCONFIG, CONF_DONE | Intel Cyclone 10 GX (U23) - Bank CSS                   | Intel Cyclone 10 Configuration signals                    |                     |
|                   | DCLK                        | Intel Cyclone 10 GX (U23) - Bank CSS<br>SPI Flash, U1  | Intel Cyclone 10<br>Configuration clock from Flash memory |                     |
|                   | MSEL0...1                   | Intel Cyclone 10 GX (U23) - Bank CSS                   | Intel Cyclone 10<br>Configuration mode signals            |                     |
|                   | DEV_CLRN, INIT_DONE         | Intel Cyclone 10 GX (U23) - Bank 2A                    |                                                           |                     |
|                   | M10_IO0...4                 | Intel Cyclone 10 GX (U23) - Bank 2A                    |                                                           |                     |
| Bank 5            | DIS_GROUP1...4              | N-Channel MOSFET, T1...4                               | Fast Discharching                                         |                     |
|                   | MAX_IO23...26               | B2B, J2                                                | Intel MAX 10 GPIO                                         |                     |
|                   | PG_0.95V, EN_0.95V          | Voltage Regulator, U7                                  | Power control signals                                     |                     |
|                   | PG_1.8VIO, EN_1.8VIO        | Voltage Regulator, U6                                  |                                                           |                     |
| Bank 6            | M10_CLK                     | 25 MHz Oscillator, U21                                 | Intel MAX 10 Clock                                        |                     |
|                   | VADJ_VS0...2, VADJ_EN       | Voltage Regulator, U11                                 | Power control signals                                     |                     |
|                   | PG_1.35V, EN_1.35V          | Voltage Regulator, U8                                  |                                                           |                     |
|                   | PG_1.8V, EN_1.8V            | Voltage Regulator, U5                                  |                                                           |                     |
|                   | PG_VTT, EN_VTT              | Voltage Regulator, U9                                  |                                                           |                     |
|                   | PG_0V9, EN_0V9              | Voltage Regulator, U4                                  |                                                           |                     |
|                   | PHY1_33LED1...2             | B2B, J2                                                | Ethernet LED                                              |                     |
|                   | LED_FP_1                    | D1                                                     | User LEDs                                                 | Red LED             |
| Bank 8            | LED_FP_2...4                | D2...4                                                 |                                                           | Green LED           |
|                   | M10_nSTATUS, M10_nCONFIG    | B2B, J2                                                | Intel MAX 10 configuration signals                        |                     |
|                   | MAX_IO1...20, 22            | B2B, J2                                                | Intel MAX 10 GPIO                                         |                     |

#### Intel MAX 10 banks information

## LEDs

| Designator | Color | Connected to | Active Level | Note |
|------------|-------|--------------|--------------|------|
| D1         | Red   | LED_FP_1     | Active high  |      |
| D2         | Green | LED_FP_2     | Active high  |      |

|    |       |          |             |  |
|----|-------|----------|-------------|--|
| D3 | Green | LED_FP_3 | Active high |  |
| D4 | Green | LED_FP_4 | Active high |  |

#### On-board LEDs

## Clock Sources

The TEI0006 has one crystal, three MEMS oscillators and a programmable clock generator.

| Designator | Description             | Frequency | Connected to         |
|------------|-------------------------|-----------|----------------------|
| U21        | MEMS Oscillator         | 25MHz     | U2 Ethernet          |
| U15        | MEMS Oscillator         | 25MHz     | IN0 of U14           |
| U17        | MEMS Oscillator         | 100 MHz   | U23, BANK2A USRCLK   |
| Y1         | Crystal Oscillator      | 50MHz     | crystal input of U14 |
| U14        | Programmable Oscillator | Variable  | -                    |

#### Oscillators

| Signals      | Clock Type   | In/ Out | Connected to                       | Frequency | Note        |
|--------------|--------------|---------|------------------------------------|-----------|-------------|
| IN0_P        | Differential | In      | Oscillator, U15                    | 25 MHz    |             |
| IN0_N        |              | In      | GND                                |           |             |
| IN3          | Differential | In      | B2B, J3                            | Variable  |             |
| XA, XB       | Differential |         | Oscillator, Y1                     | 50 MHz    |             |
| CLK0         | Differential | Out     | Intel Cyclone 10 GX (U23)- Bank 2A | User      | Default off |
| CLK1...4     | Differential | Out     | B2B, J3                            | User      | Default off |
| REFCLK_EMIFP | Differential | Out     | Intel Cyclon 10 GX (U23)- Bank 3B  | User      | Default off |
| CLK6...7     | Differential | Out     | Intel Cyclon 10 GX (U23)- Bank 1D  | User      | Default off |
| CLK8...9     | Differential | Out     | Intel Cyclon 10 GX (U23)- Bank 1C  | User      | Default off |

#### Programmable Oscillator connections

## CryptoAuthentication

ATECC608A (U19) is a CryptoAuthentication device connected to the I<sup>2</sup>C bus. This chip is optional, for further description see datasheet of manufacturer.

| Schematic | U19 Pin | B2B    | U18 Intel Max 10 Pin | Notes |
|-----------|---------|--------|----------------------|-------|
| I2C_SCL   | SCL     | J3-135 | Bank 2 - K2          | -     |
| I2C_SDA   | SDA     | J3-137 | Bank 2 - L2          | -     |

#### I2C Interface of CryptoAuthentication

## Power and Power-On Sequence

## Power Supply

Power supply with minimum current capability of 1 A for system startup is recommended.

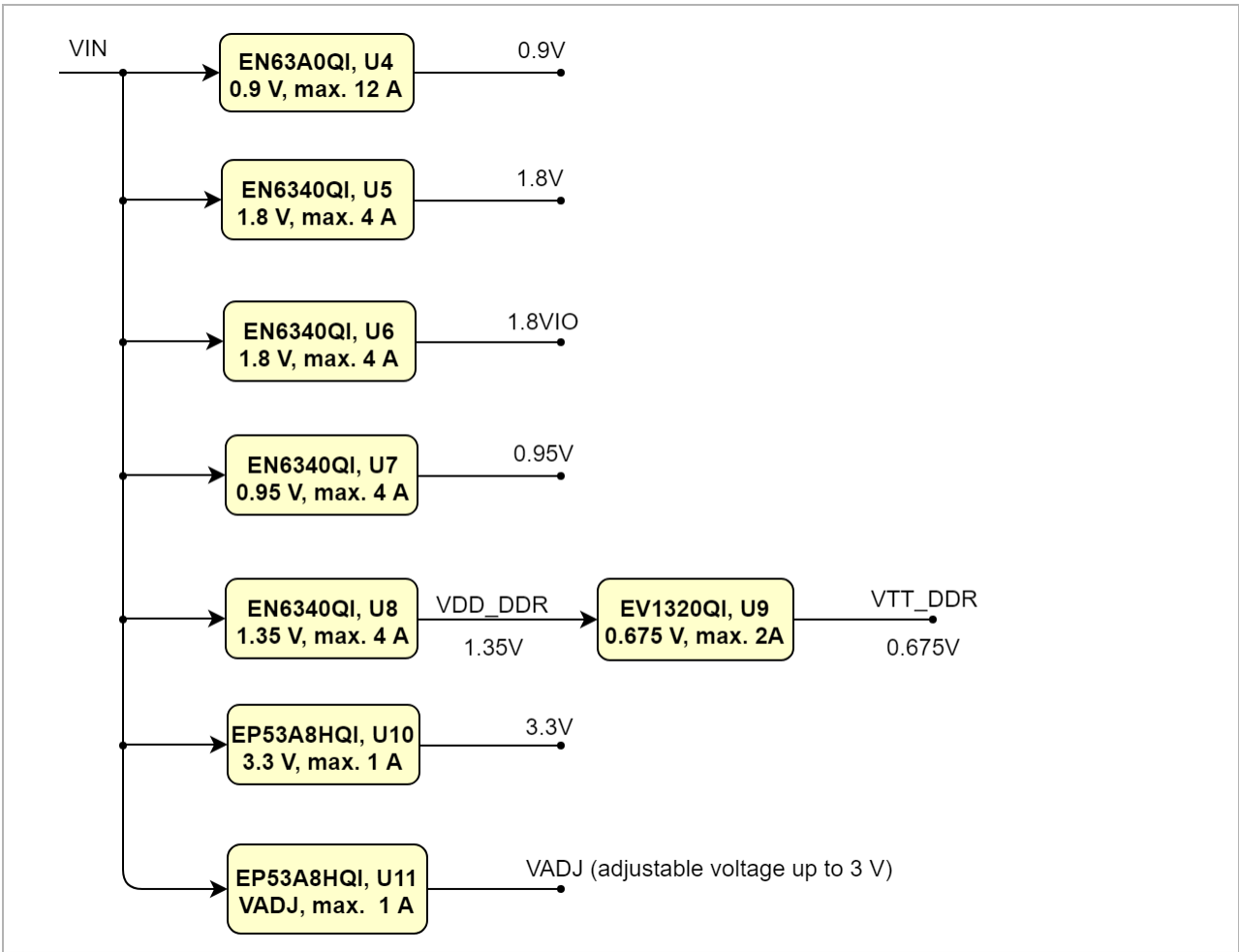
## Power Consumption

| FPGA                | Typical Current |
|---------------------|-----------------|
| Intel Cyclone 10 GX | TBD*            |
| Intel MAX 10        | TBD*            |

**Power Consumption**

\* TBD - To Be Determined

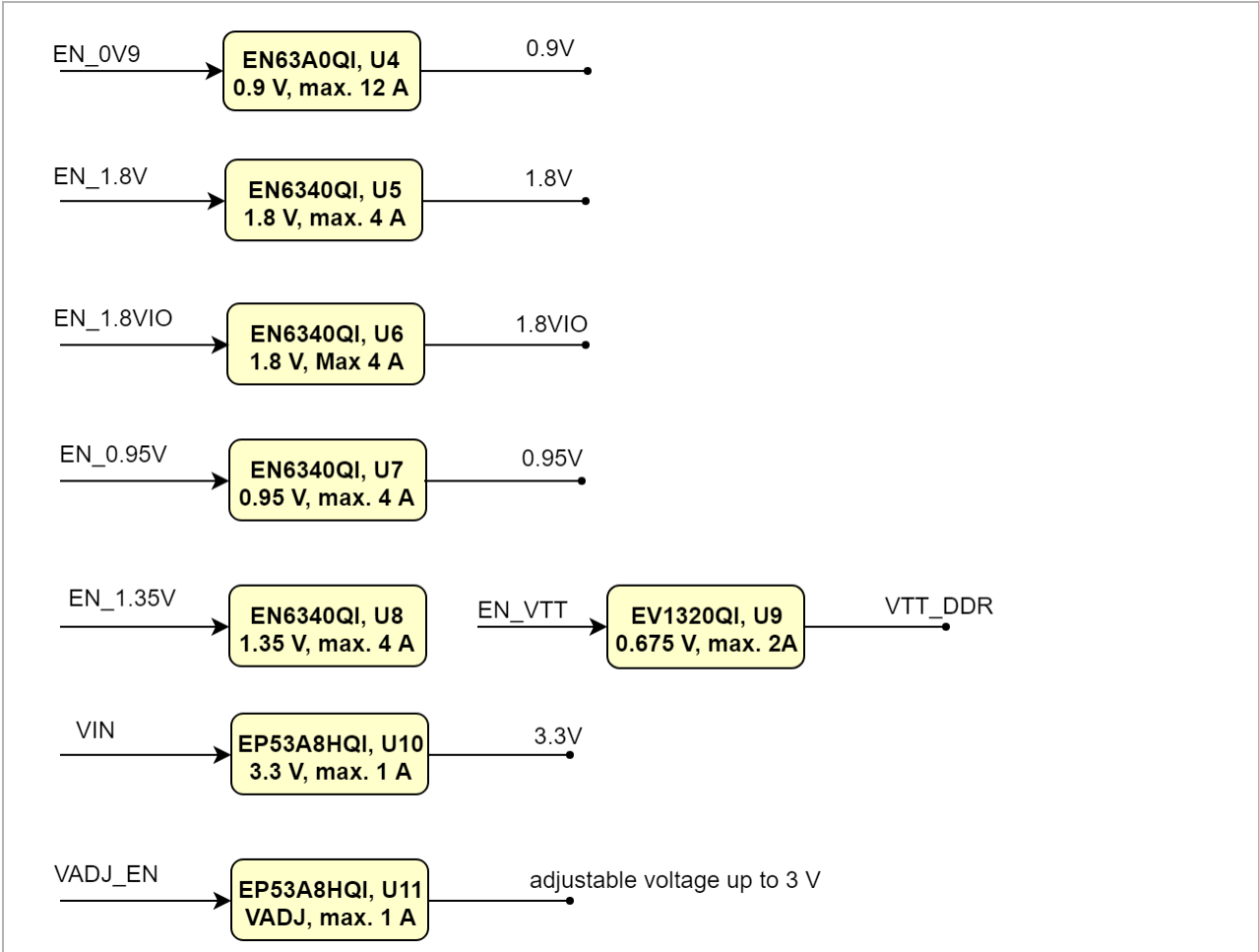
## Power Distribution Dependencies



Power Distribution

## Power-On Sequence

Voltage regulators can be enabled through U18 (Intel MAX 10) - Bank 5 and 6.



Power Sequence

Power Rails

| Power Rail Name | B2B Connector J1 Pin                  | B2B Connector J2 Pin | B2B Connector J3 Pin | Voltage Level                         | Direction | Notes                                                                            |
|-----------------|---------------------------------------|----------------------|----------------------|---------------------------------------|-----------|----------------------------------------------------------------------------------|
| VIN             | 145, 147,149, 151, 153, 155, 157, 159 | -                    | -                    | 5 V                                   | Input     |                                                                                  |
| VCCIO2K         | 53, 54                                | -                    | -                    | 1.2 V, 1.25 V, 1.35 V, 1.5 V or 1.8 V | Input     |                                                                                  |
| VADJ            | 140,142                               | -                    | -                    | adjustable between 1.8 V - 3.0 V      | Output    | Voltages according to EP53A8HQI datasheet but restricted to allowed bank voltage |
| VCCIO2J         | -                                     | 29,30                | -                    | 1.2 V, 1.25 V, 1.35 V, 1.5 V or 1.8 V | Input     |                                                                                  |
| 3.3V            | -                                     | 149,150              | -                    | 3.3 V                                 | Output    |                                                                                  |

|         |   |   |     |       |        |  |
|---------|---|---|-----|-------|--------|--|
| 1.8_VIO | - | - | 139 | 1.8 V | Output |  |
|---------|---|---|-----|-------|--------|--|

Module power rails.

## Bank Voltages

| FPGA                | FPGA Bank | Voltage Level                         | Notes                                     |
|---------------------|-----------|---------------------------------------|-------------------------------------------|
| Intel Cyclone 10 GX | Bank 1C   | 0.95 V                                |                                           |
|                     | Bank 1D   | 0.95 V                                |                                           |
|                     | Bank 2A   | 1.8 V                                 | 1.8VIO                                    |
|                     | Bank 2J   | 1.2 V, 1.25 V, 1.35 V, 1.5 V or 1.8 V | VCCIO2J                                   |
|                     | Bank 2K   | 1.2 V, 1.25 V, 1.35 V, 1.5 V or 1.8 V | VCCIO2K                                   |
|                     | Bank 2L   | adjustable between 1.8 V - 3.0 V      | Voltages according to EP53A8HQI datasheet |
|                     | Bank 3A   | 1.35 V                                | VDD_DDR                                   |
|                     | Bank 3B   | 1.35 V                                | VDD_DDR                                   |
| Intel Max 10        | Bank 1A   | 3.3 V                                 |                                           |
|                     | Bank 1B   | 3.3 V                                 |                                           |
|                     | Bank 2    | 1.8 V                                 | 1.8VIO                                    |
|                     | Bank 3    | 1.8 V                                 | 1.8VIO                                    |
|                     | Bank 5    | 3.3V                                  |                                           |
|                     | Bank 6    | 3.3V                                  |                                           |
|                     | Bank 8    | 3.3V                                  |                                           |

SoC bank voltages.

## Board to Board Connectors

The module has three 160-pin double-row REF-192552-02 connector on the bottom side. The counterpart REF-192552-01 is placed on the base board.

| Order number | REF Number    | Samtec Number        | Type                | Mated Height | Data sheet                                                                                                              | Comment                           |
|--------------|---------------|----------------------|---------------------|--------------|-------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| 27220        | REF-192552-02 | ST5-80-1.50-L-D-P-TR | Module connector    | 5 mm         | <a href="http://suddendocs.samtec.com/catalog_english/st5.pdf">http://suddendocs.samtec.com/catalog_english/st5.pdf</a> | Standard connector used on module |
| 27219        | REF-192552-01 | SS5-80-3.50-L-D-K-TR | Baseboard connector | 5 mm         | <a href="http://suddendocs.samtec.com/catalog_english/ss5.pdf">http://suddendocs.samtec.com/catalog_english/ss5.pdf</a> | Standard connector used on board  |

Connectors.

With different connectors from the used series other mating heights are possible (according to the [Datasheet](#)). The module and base board can be manufactured using other connectors upon request.

| Connector Specifications | Value                  |
|--------------------------|------------------------|
| Insulator material       | Liquid crystal polymer |
| Stacking height          | 5 mm                   |

|                             |                                |
|-----------------------------|--------------------------------|
| Contact material            | Phosphor-bronze                |
| Plating                     | Au or Sn over 50 " (1.27 m) Ni |
| Current rating              | 1.6 A per pin (2 pins powered) |
| Operating temperature range | -55 °C to +125 °C              |
| RoHS compliant              | Yes                            |

#### Connector specifications.

#### Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

| Stacking height    | Speed rating     |
|--------------------|------------------|
| 5 mm, Single-Ended | 13.5GHz / 27Gbps |
| 5 mm, Differential | 20GHz / 40Gbps   |
| 4 mm, Single-Ended | 13GHz / 26Gbps   |
| 4 mm, Differential | 13.5GHz / 27Gbps |

#### Speed rating.

#### Current Rating

Current rating of Samtec Razor Beam™ SS5/ST5 B2B connectors is 1.6A per pin (2 pins powered).

#### Connector Mechanical Ratings

- Shock: 100G, 6 ms sawtooth wave
- Vibration: 7.56G 'RMS', 2 hours per axis, 3 axes total

#### Manufacturer Documentation

| File                                         | Modified                     |
|----------------------------------------------|------------------------------|
| PDF File hsc-report-sma_st5-ss5-04mm_web.pdf | 07 06, 2019 by John Hartfiel |
| PDF File hsc-report-sma_st5-ss5-05mm_web.pdf | 07 06, 2019 by John Hartfiel |
| PDF File ss5_catalog.pdf                     | 07 06, 2019 by John Hartfiel |
| PDF File ss5-st5_specs.pdf                   | 07 06, 2019 by John Hartfiel |

[Download All](#)

## Technical Specifications

## Absolute Maximum Ratings

| Symbols          | Description              | Min  | Max  | Unit | Note                |
|------------------|--------------------------|------|------|------|---------------------|
| VIN              | Power supply             | -0.3 | 6.0  | V    | Determined by U10.  |
| VCCIO - 3 V I/O  | I/O buffers power supply | -0.5 | 4.10 | V    | Intel Cyclone 10 GX |
| VCCIO - LVDS I/O | I/O buffers power supply | -0.5 | 2.46 | V    | Intel Cyclone 10 GX |
| VADJ             | Adjustable voltage       | -0.5 | 4.10 | V    | Intel Cyclone 10 GX |
| T_STG            | Storage temperature      | -40  | 85   | °C   |                     |

#### Absolute maximum ratings

## Recommended Operating Conditions

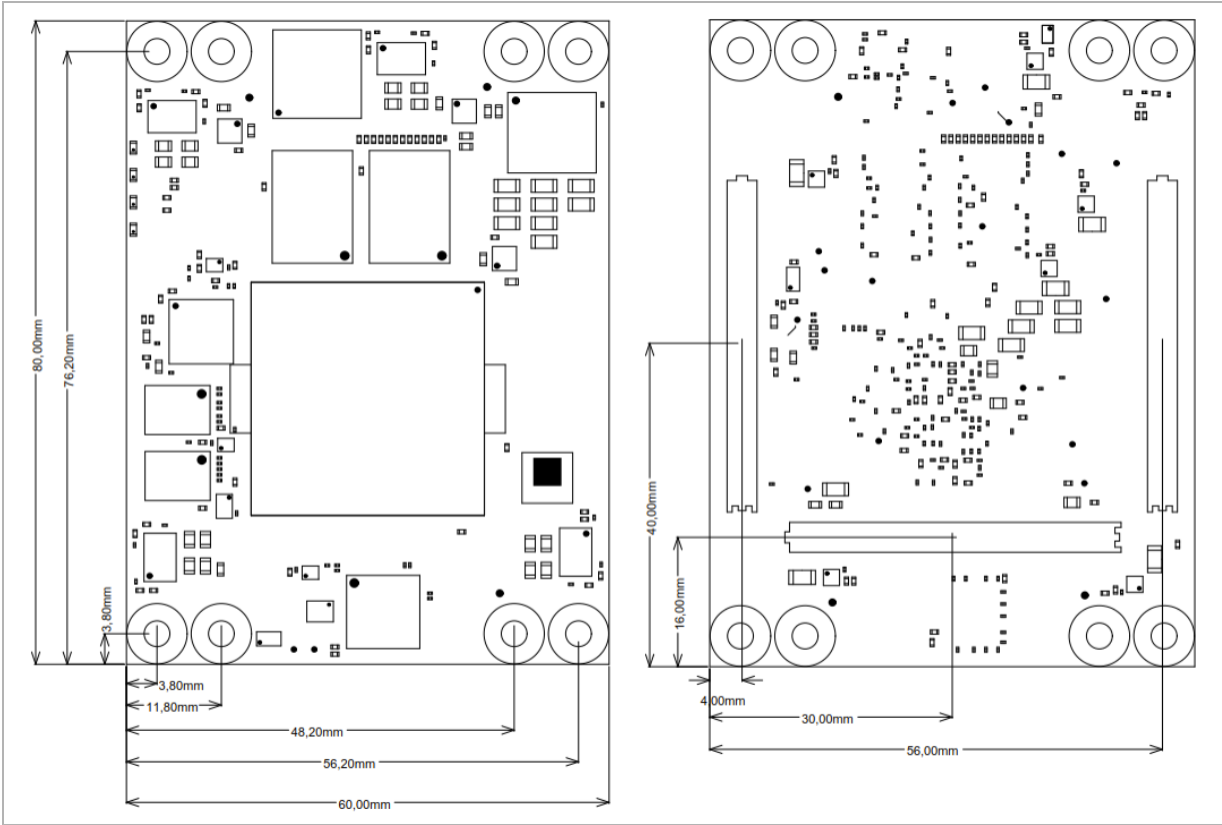
Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

| Parameter | Min  | Max  | Unit | Reference Document                 |
|-----------|------|------|------|------------------------------------|
| VIN       | 5.0  | 5.0  | V    |                                    |
| VCCIO     | 2.85 | 3.15 | V    | See Intel Cyclone 10 GX datasheet. |
| VADJ      | 2.85 | 3.15 | V    | VCCIO                              |

#### Recommended operating conditions.

## Physical Dimensions

- Module size: 60 mm × 80 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 5 mm.
- PCB thickness: 1.7 mm



Physical Dimension

## Currently Offered Variants

|                                  |                             |
|----------------------------------|-----------------------------|
| Trenz shop TEI0006 overview page |                             |
| <a href="#">English page</a>     | <a href="#">German page</a> |

Trenz Electronic Shop Overview

## Revision History

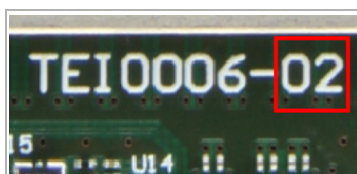
### Hardware Revision History

| Date      | Revision | Changes                                                                                                          | Documentation Link    |
|-----------|----------|------------------------------------------------------------------------------------------------------------------|-----------------------|
| 202-12-23 | 03       | <ul style="list-style-type: none"><li>two input clock signals on B2B connected directly to GXBL1C bank</li></ul> | <a href="#">REV03</a> |

|            |    |                                                                                                                                                                                                                                                                                                                    |                       |
|------------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| 2019-09-11 | 02 | <ul style="list-style-type: none"> <li>added 100MHz MEMS oscillator, remove CLKUSR signal from J2</li> <li>replaced U21/U15 by SiT8008</li> <li>added pull-up to M10_NSTATUS signal</li> <li>added pull-up to M10_DEVCLRN, removed signal from J2</li> <li>added optional CryptoAuthentication chip U19</li> </ul> | <a href="#">REV02</a> |
| 2018-08-10 | 01 | -                                                                                                                                                                                                                                                                                                                  | <a href="#">REV01</a> |

#### Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board hardware revision number.

## Document Change History

| Date | Revision | Contributor | Description |
|------|----------|-------------|-------------|
|------|----------|-------------|-------------|

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> | <ul style="list-style-type: none"> <li>corrected Bank Voltages for Bank 2J (VCCIO2 J) and Bank 2K (VCCIO2 K)</li> </ul> |
| 2022-03-18                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | v.85                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Vitali Tsiukala                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | <ul style="list-style-type: none"> <li>Added Info about Gigabit Transceivers</li> </ul>                                 |
| 2021-06-07                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | v.84                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Martin Rohrmüller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>corrected Physical Dimension figure</li> <li>updated to REV03</li> </ul>         |
| 2020-01-17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | v.82                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Martin Rohrmüller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>updated to REV02</li> </ul>                                                      |

|            |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                             |
|------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| 2019-06-14 | v.80 | Pedram Babakhani                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"> <li>Figures updated</li> <li>Technical specifications updated</li> </ul> |
| 2019-05-29 | v.69 | Pedram Babakhani                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <ul style="list-style-type: none"> <li>initial release</li> </ul>                                           |
| --         | all  | <div> <p><b>Error rendering macro 'page-info'</b></p> <p>Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</p> </div> | <ul style="list-style-type: none"> <li>--</li> </ul>                                                        |

Document change history.

## Disclaimer

## Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

## Document Warranty

The material contained in this document is provided "as is" and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

## Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

## Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

## Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

## Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## REACH, RoHS and WEEE

### REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

### RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

### WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

**Error rendering macro 'page-info'**

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`