TEI0009 RISC-V SCR1 Demo

This project is Syntacore SCR1 RISC-V based SoC demo for Cyclone 10LP Refkit. The complete project is based on Syntacore SCR1 SDK from github. C10LP Refkit support is added by changes to two subprojects of of Syntacore scr1-sdk github

Github fork	Description
https://github.com/micro-FPGA/fpga-sdk-prj	Quartus project for C10LP Refkit added
https://github.com/micro-FPGA/sc-bl	Syntacore RISC-V bootloader

Build instructions

Clone Syntacore main scr1-sdk github, then fetch both forks and merge, then compile.

Quartus version used 18.1

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