

# TE0820 Test Board

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### Revision History

Date	Authors	Description
2024-03-05	Manuela Strücker	<ul style="list-style-type: none"><li>bugfix file_location.txt</li><li>update USB available in uboot</li></ul>
2024-02-23	Manuela Strücker	<ul style="list-style-type: none"><li>2023.2 release</li><li>new assembly variants</li></ul>
2023-06-22	Manuela Strücker	<ul style="list-style-type: none"><li>2022.2 release</li><li>new assembly variants</li></ul>

2023-03-24	2021.2.1	TE0820-test_board-vivado_2021.2-build_20_20230324121549.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_20_20230324121549.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2022-09-28	2021.2.1	TE0820-test_board-vivado_2021.2-build_17_20220928065907.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_17_20220928065907.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>bugfix fsbl generation</li> <li>new assembly variants</li> </ul>
2022-09-12	2021.2.1	TE0820-test_board-vivado_2021.2-build_15_20220912132233.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_15_20220912132233.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>update board part files compatible to Vivado 2021.2.1</li> <li>new assembly variants</li> </ul>
2022-01-28	2021.2	TE0820-test_board-vivado_2021.2-build_11_20220128090819.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_11_20220128090819.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2022-01-24	2021.2	TE0820-test_board-vivado_2021.2-build_10_20220124111148.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_10_20220124111148.zip	John Hartfiel	<ul style="list-style-type: none"> <li>adding missing u-boot device tree to the boot.bin</li> </ul>
2022-01-14	2021.2	TE0820-test_board-vivado_2021.2-build_8_20220114123035.zip TE0820-test_board_noprebuilt-vivado_2021.2-build_8_20220114123035.zip	John Hartfiel	<ul style="list-style-type: none"> <li>2021.2 release</li> <li>new assembly variants</li> <li>remove alle PCB Revision 02 variant with 1GB DDR</li> </ul>
2021-06-01	2020.2	TE0820-test_board-vivado_2020.2-build_5_20210601084124.zip TE0820-test_board_noprebuilt-vivado_2020.2-build_5_20210601092528.zip	John Hartfiel	<ul style="list-style-type: none"> <li>2020.2 release</li> <li>new assembly variants</li> </ul>

2020-04-08	2019.2	TE0820-test_board_noprebui lt-vivado_2019.2- build_10_20200408 073458.zip TE0820-test_board- vivado_2019.2- build_10_20200408 073444.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• script update</li> <li>• new assembly variants</li> </ul>
2020-03-25	2019.2	TE0820-test_board_noprebui lt-vivado_2019.2- build_8_202003250 83817.zip TE0820-test_board- vivado_2019.2- build_8_202003250 83750.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• script update</li> <li>• Board Part update (minor changes)</li> </ul>
2020-01-22	2019.2	TE0820-test_board_noprebui lt-vivado_2019.2- build_3_202001221 54341.zip TE0820-test_board- vivado_2019.2- build_3_202001221 54318.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• script update for linux user</li> </ul>
2020-01-14	2019.2	TE0820-test_board- vivado_2019.2- build_3_202001140 81551.zip TE0820- test_board_noprebui lt-vivado_2019.2- build_3_202001140 81612.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• add fsbl_flash binary</li> <li>• Vitis script updates (include linux domain and prebuilt linux files for vitis)</li> <li>• prebuilt binary export on selection guide</li> </ul>
2019-12-19	2019.2	TE0820-test_board- vivado_2019.2- build_1_201912190 75647.zip TE0820- test_board_noprebui lt-vivado_2019.2- build_1_201912190 80228.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• 2019.2 update</li> <li>• Vitis support</li> </ul>
2019-10-29	2018.3	TE0820-test_board_noprebui lt-vivado_2018.3- build_09_20191029 071045.zip TE0820-test_board- vivado_2018.3- build_09_20191029 071028.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2019-08-09	2018.3	TE0820-test_board_noprebui lt-vivado_2018.3- build_07_20190809 084040.zip TE0820-test_board- vivado_2018.3- build_07_20190809 083901.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix fsbl (removed second PSU init)</li> </ul>

2019-06-19	2018.3	TE0820-test_board_noprebui lt-vivado_2018.3- build_06_20190619 073300.zip TE0820-test_board- vivado_2018.3- build_06_20190619 073243.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> <li>• USB2 only (change PS IP and device tree)</li> <li>• FSBL changes</li> </ul>
2019-04-01	2018.3	TE0820-test_board_noprebui lt-vivado_2018.3- build_03_20190401 130135.zip TE0820-test_board- vivado_2018.3- build_03_20190401 130123.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• renamed ...D variants to ...A</li> </ul>
2019-02-21	2018.3	TE0820-test_board_noprebui lt-vivado_2018.3- build_01_20190221 103025.zip TE0820-test_board- vivado_2018.3- build_01_20190221 102913.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• TE Script update</li> <li>• rework of the FSBLs</li> <li>• SI5338 CLKBuilder Pro Project</li> <li>• some additional Linux features</li> <li>• MAC from EEPROM</li> <li>• new assembly variants</li> <li>• remove special compiler flags, which was needed in 2018.2</li> </ul>
2018-10-31	2018.2	TE0820-test_board_noprebui lt-vivado_2018.2- build_03_20181031 164506.zip  TE0820-test_board- vivado_2018.2- build_03_20181031 164452.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> <li>• update optional petalinux startup init script</li> </ul>
2018-09-12	2018.2	TE0820-test_board_noprebui lt-vivado_2018.2- build_03_20180912 094615.zip TE0820-test_board- vivado_2018.2- build_03_20180912 094558.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• correction: <ul style="list-style-type: none"> <li>◦ TE0820-03-4EV-1EA has 2GB DDR, now 2GB instead of 1GB is initialised</li> <li>◦ small changes on DDR setup of TE0820-02-2EG-1EE</li> </ul> </li> </ul>

2018-08-15	2018.2	TE0820-test_board-vivado_2018.2-build_01_20180706212937.zip TE0820-test_board_noprebuilt-vivado_2018.2-build_01_20180706212952.zip	John Hartfiel	<ul style="list-style-type: none"> <li>different design for REV03</li> <li>small petalinux changes</li> <li>IO renaming</li> <li>additional notes for FSBL generated with Win SDK</li> <li>changed *.bif</li> </ul>
2018-06-19	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180619160728.zip	John Hartfiel	<ul style="list-style-type: none"> <li>bugfix board part files BANK1 MIO voltages</li> <li>Add "dummy" PS USB3 parameter so solve problems with some USB2 devices</li> </ul>
2018-05-24	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180524151342.zip	John Hartfiel	<ul style="list-style-type: none"> <li>solved Linux Flash issue</li> <li>new assembly variant</li> </ul>
2018-04-25	2017.4	TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_07_20180425134459.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2018-02-06	2017.4	TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_06_20180206203414.zip	John Hartfiel	<ul style="list-style-type: none"> <li>solved JTAG /Linux issue</li> </ul>
2018-02-01	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180201084319.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180201094724.zip	John Hartfiel	<ul style="list-style-type: none"> <li>board part csv update</li> </ul>

2018-01-24	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180124085303.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• rework board part files</li> <li>• solved USB, QSPI and PHY issue</li> </ul>
2017-11-21	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171121160552.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171121160606.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• solved SD SDX Cards Problem</li> <li>• Separate csv name for all assembly variants</li> </ul>
2017-11-20	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171120162931.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171120162851.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• solved SD WP Problem</li> </ul>
2017-10-19	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171019104824.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171019104837.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• initial release</li> </ul>

**Design Revision History**

## Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Uboot: Ethernet not present	Ethernet in Uboot cannot be used due to no MAC address set (Error: ethernet@ff0e0000 address not set.)	please set CONFIG_NET_RANDOM_ETHADDR in petalinux-config -c u-boot  as a side effect, MAC address will be random in Linux also	2023.2 version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see <a href="#">Xilinx Forum Request</a>	use corresponding board files for the Vivado versions	--
Uboot did not start	Effected Design: TE0820-test_board-vivado_2020.2-build_5_20210601084124.zip TE0820-test_board_noprebuilt-vivado_2020.2-build_5_20210601092528.zip	Use older version, this will be fixed as soon as possible	<b>Solved</b> with 20220124 update

Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible "jedec,spi-nor""	<b>Solved</b> with 20180524 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is necessary:  <ol style="list-style-type: none"> <li>1. Boot linux with usb terminal</li> <li>2. From the terminal: root root mount ifconfig eth0</li> <li>3. Open two new SSH terminals via ethernet: root root , run user application ...</li> <li>4. Exit and close the usb terminal</li> </ol>	<b>Solved</b> with 20180206 update

#### Known Issues

## Requirements

### Software

Software	Version	Note
Vitis	2023.2	needed, Vivado is included into Vitis installation
PetaLinux	2023.2	needed
SI ClockBuilder Pro	---	optional

#### Software

### Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on "<project folder>\board\_files\\*\_board\_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
<del>TE0820-ES4</del>	<del>es4</del>	<del>REV04</del>	<del>4GB</del>	<del>64MB</del>	<del>4GB</del>	<del>NA</del>	<del>Not longer supported by vivado</del>
<del>TE0820-02-02CG-4E</del>	<del>2eg_1e_1gb</del>	<del>REV02</del>	<del>4GB</del>	<del>64MB</del>	<del>4GB</del>	<del>NA</del>	<del>Not longer supported- use 2020.2 or older</del>
<del>TE0820-02-02CG-4EA</del>	<del>2eg_1e_1gb</del>	<del>REV02</del>	<del>4GB</del>	<del>128MB</del>	<del>4GB</del>	<del>NA</del>	<del>Not longer supported- use 2020.2 or older</del>
<del>TE0820-02-02EG-4E</del>	<del>2eg_1e_1gb</del>	<del>REV02</del>	<del>4GB</del>	<del>64MB</del>	<del>4GB</del>	<del>NA</del>	<del>Not longer supported- use 2020.2 or older</del>

TE0820-02-02EG-1E3	2eg_1e_1gb	REV02	4GB	64MB	4GB	2.5 mm-connectors	Not longer-supported-use 2020.2 or older
TE0820-02-02EG-1EA	2eg_1e_1gb	REV02	4GB	128MB	4GB	NA	Not longer-supported-use 2020.2 or older
TE0820-02-02EG-1EL	2eg_1e_1gb	REV02	4GB	128MB	4GB	2.5 mm-connectors	Not longer-supported-use 2020.2 or older
TE0820-02-03CG-1E	3eg_1e_1gb	REV02	4GB	64MB	4GB	NA	Not longer-supported-use 2020.2 or older
TE0820-02-03CG-1EA	3eg_1e_1gb	REV02	4GB	128MB	4GB	NA	Not longer-supported-use 2020.2 or older
TE0820-02-03EG-1E	3eg_1e_1gb	REV02	4GB	64MB	4GB	NA	Not longer-supported-use 2020.2 or older
TE0820-02-03EG-1E3	3eg_1e_1gb	REV02	4GB	64MB	4GB	2.5 mm-connectors	Not longer-supported-use 2020.2 or older
TE0820-02-03EG-1EA	3eg_1e_1gb	REV02	4GB	128MB	4GB	NA	Not longer-supported-use 2020.2 or older
TE0820-02-03EG-1EL	3eg_1e_1gb	REV02	4GB	128MB	4GB	2.5 mm-connectors	Not longer-supported-use 2020.2 or older
TE0820-02-04CG-1EA	4eg_1e_1gb	REV02	4GB	128MB	4GB	NA	Not longer-supported-use 2020.2 or older
TE0820-03-02CG-1EA	2cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02CG-1ED	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-02EG-1EA	2eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EL	2eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-03CG-1EA	3cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-04CG-1EA	4cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-04EV-1EA	4ev_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-2AE21FA	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2AI21FA	2cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FA	2eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FL	2eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA



TE0820-03-2BI21FA	2eg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BI21FL	2eg_1i_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-3AE21FA	3cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AI210A	3cg_1i_2gb	REV03	2GB	128MB	0GB	NA	NA
TE0820-03-3AI21FA	3cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3BE21FA	3eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3BE21FL	3eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-4AE21FA	4cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4AI21FI	4cg_1i_x_2gb	REV03	2GB	128MB	8GB	without ETH PHY	NA
TE0820-03-4DE21FA	4ev_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FC	4ev_1e_2gb	REV03	2GB	128MB	8GB	without encryption NCNR	NA
TE0820-03-4DE21FL	4ev_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-4DI21FA	4ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-5DI21FA	5ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-5DR21FA	5ev_1q_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-04-2AE21FA	2cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2AI21FA	2cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2AI21MC	2cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21-V1	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	Customised
TE0820-04-2BE21FA	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21FAJ	2eg_1e_2gb	REV04	2GB	128MB	8GB	without spacers	NA
TE0820-04-2BE21FL	2eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-2BE21MA	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21MAJ	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21FA	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21FL	2eg_1i_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-2BI21MA	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21ML	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AE21FA	3cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AE21MA	3cg_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr

TE0820-04-3AI21FA	3cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AI21FAT	3cg_1i_2gb	REV04	2GB	128MB	8GB	NA	Customer supplied
TE0820-04-3BE21FA	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3BE21FL	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-3BE21KA	3eg_1e_2gb	REV04	2GB	128MB	64GB	NA	NA
TE0820-04-3BE21MA	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3BE21ML	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-3BE21MLZ	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-4AE21FA	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4AE21MA	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4AI21FI	4cg_1i_x_2gb	REV04	2GB	128MB	8GB	without ETH PHY	NA
TE0820-04-4BI21KL	4eg_1i_2gb	REV04	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-04-4DE21FA	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4DE21FL	4ev_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-4DE21MA	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-04-4DI21FA	4ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4DI21MA	4ev_1i_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-04-5DI21FA	5ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-5DI21MA	5ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-5DR21FA	5ev_1q_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-S002	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr Custom supplied TE0820-04-3BE21MA
TE0820-04-S002C1	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO
TE0820-04-S003	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-S004	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO
TE0820-04-S005	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	Other EMMC mfr Custom supplied TE0820-04-4AE21MA
TE0820-04-S006	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO:Other EMMC mfr
TE0820-04-S009	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-04-S010	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO:Other EMMC mfr

TE0820-04-S013	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	CAO:Other EMMC mfr
TE0820-04-S016	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	CAO:Other EMMC mfr
TE0820-04-S018	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	CAO
TE0820-05-2AE21MA	2cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AE21MAZ	2cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AE81MA	2cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AI21MA	2cg_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2AI81MA	2cg_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BE21MA	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BE21MAJ	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BI21MA	2eg_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-2BI81ML	2eg_1i_2gb	REV05	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-05-3AE21MA	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3AE81MA	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE21MA	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE21MAZ	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE81MA	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-3BE81ML	3eg_1e_2gb	REV05	2GB	128MB	8GB	2.5 mm connectors	Other EMMC mfr
TE0820-05-3BI21ML	3eg_1i_2gb	REV05	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-05-4AE21MA	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-4AE81MA	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-4AI21MI	4cg_1i_x_2gb	REV05	2GB	128MB	8GB	without ETH PHY	NA
TE0820-05-4BI21PL	4eg_1i_2gb	REV05	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-05-4BI21PLZ	4eg_1i_2gb	REV05	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-05-4DE21MA	4ev_1e_2gb	REV05	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-05-4DI21MA	4ev_1i_2gb	REV05	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-05-4DI81MA	4ev_1i_2gb	REV05	2GB	128MB	8GB	NA	Other EMMC mfr
TE0820-05-5DI21MA	5ev_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-5DI81MA	5ev_1i_2gb	REV05	2GB	128MB	8GB	NA	NA
TE0820-05-S002C1	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO

TE0820-05-S003	4ev_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S004C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S005	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S008C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO:without PLL
TE0820-05-S013	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO:without PLL
TE0820-05-S014C1	4cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S016	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S017C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO:without PLL
TE0820-05-S018	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S020	3eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S022	3cg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO
TE0820-05-S024C1	2eg_1e_2gb	REV05	2GB	128MB	8GB	NA	CAO

\*used as reference

#### Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 SoM Carriers</a></li> </ul>
TE0703*	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 cm carriers</a></li> <li>Used as reference carrier.</li> </ul>
TE0705	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 SoM Carriers</a></li> </ul>
TE0706	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 SoM Carriers</a></li> </ul>
TEB0707	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 SoM Carriers</a></li> </ul>

TEBA0841	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 SoM Carriers</a></li> <li>No SD Slot available, pins goes to Pin Header</li> <li>For TEBA0841 REV01, please contact TE support</li> </ul>
TEF1002	<ul style="list-style-type: none"> <li>Important: See restrictions on usage with 7 Serie Carriers: <a href="#">4 x 5 SoM Carriers</a></li> </ul>

\*used as reference

#### Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

#### Additional Hardware

## Content

For general structure and of the reference design, see [Project Delivery - AMD devices](#)

## Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

#### Design sources

## Additional Sources

Type	Location	Notes
------	----------	-------

SI5338	<project folder>\misc\SI5338	SI5338 Project with current PLL Configuration
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

#### Additional design sources

## Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado <a href="#">hardware description file</a> for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

#### Prebuilt files (only on ZIP with prebuilt content)

## Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0820 "Test Board" Reference Design](#)

## Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects - TE Reference Design](#)
- [Project Delivery](#).

The Trenez Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)



**Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

#### **\_create\_win\_setup.cmd/\_create\_linux\_setup.sh**

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference
Design-----
-----
-- (0) Module selection guide, project creation...prebuilt export...
-- (1) Create minimum setup of CMD-Files and exit Batch
-- (2) Create maximum setup of CMD-Files and exit Batch
-- (3) (internal only) Dev
-- (4) (internal only) Prod
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (g) Install Board Files from Xilinx Board Store (beta)
-- (a) Start design with unsupported Vivado Version (beta)
-- (x) Exit Batch (nothing is done!)
----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
  - optional for manual changes: Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_guiemode.cmd"




Note: Select correct one, see also [Vivado Board Part Flow](#)


4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

**run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")**

```
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.


5. Create and configure your PetaLinux project with exported .xsa-file, see [PetaLinux KICKstart](#)
  - use TE Template from "<project folder>\os\petalinux"
  - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>". **Note:** HW Export from Vivado GUI creates another path as default workspace.
6. Configure the **boot.scr** file as needed, see [Distro Boot with Boot.scr](#)
7. Generate Programming Files with Vitis
  - a. Copy PetaLinux build image files to prebuilt folder
    - i. copy **u-boot.elf**, **system.dtb**, **bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

 "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

- b. Generate Programming Files

**run on Vivado TCL (Script generates applications and bootable files, which are defined in "test\_board\sw\_lib\apps\_list.csv")**


```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or
start with TE Scripts on Vivado TCL)
```

 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)

8. Generate Programming Files with Petalinux (alternative), see [PetaLinux KICKstart](#)

## Launch

## Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

## Get prebuilt boot binaries

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell:
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection



- c. Select create and open delivery binary folder



Note: Folder "<project folder>/\_binaries\_<Article Name>" with subfolder "boot\_<app name>" for different applications will be generated

## QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub**, and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado\_open\_existing\_project\_gui mode.cmd" or if not created, create with "vivado\_create\_project\_gui mode.cmd"

### run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

```
TE::pr_program_flash -swapp u-boot  
TE::pr_program_flash -swapp hello_te0820 (optional)
```



To program with Vitis/Vivado GUI, use special FSBL (fsbl\_flash) on setup

3. Copy **image.ub**, and **boot.scr** on **SD** or **USB**
  - use files from "<project folder>\\_binaries\_<Article Name>\boot\_linux" from generated binary folder, see: [Get prebuilt boot binaries](#)
  - or use prebuilt file location, see "<project folder>\prebuilt\file\_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
  - Depends on Carrier, see carrier TRM.

## SD-Boot mode

1. Copy **image.ub**, **boot.scr** and **Boot.bin** on **SD**
  - use files from "<project folder>\\_binaries\_<Article Name>\boot\_linux" from generated binary folder, see: [Get prebuilt boot binaries](#)
  - or use prebuilt file location, see "<project folder>\prebuilt\file\_location.txt"
2. Set Boot Mode to SD-Boot.
  - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

## JTAG

Not used on this example.

## Usage

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)



Note: See TRM of the Carrier, which is used.



Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.

The boot options described above describe the common boot processes for this hardware; other boot options are possible.

For more information see [Distro Boot with Boot.scr](#)

#### 4. Power On PCB

1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,
2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,
3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

## Linux

#### 1. Open Serial Console (e.g. putty)

- Speed: 115200
- select COM Port



Win OS, see device manager, Linux OS see dmesg |grep tty (UART is \*USB1)

#### 2. Linux Console:



Note: Wait until Linux boot finished

#### 3. You can use Linux shell now.

```
i2cdetect -y -r 0      (check I2C 0 Bus)
dmesg | grep rtc       (RTC check)
udhcpc                 (ETH0 check)
lsusb                  (USB check)
```

#### 4. Option Features

- Webserver to get access to Zynq
  - insert IP on web browser to start web interface
- init.sh scripts
  - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

## Vivado HW Manager

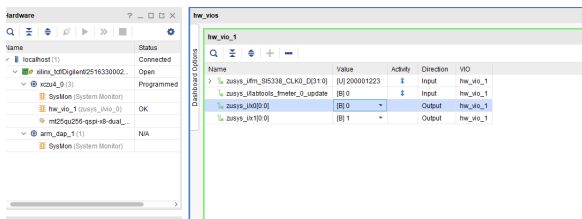
Open Vivado HW-Manager and add VIO signal to dashboard (\*.ltx located on prebuilt folder)

- Control:
  - User LED (PCB REV03 and newer)
- Monitoring:
  - SI5338\_CLK0 Counter:

- Set radix from VIO signals to unsigned integer.  
Note: Frequency Counter is inaccurate and displayed unit is Hz
- SI5338 CLK is configured to 200MHz by default.

PCB REV03 Design:

- User LED, see: [TE0820 CPLD#LED](#)

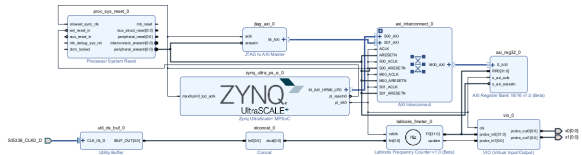


Vivado Hardware Manager

# System Design - Vivado

## Block Design

### PCB REV03



Block Design PCB REV03

## PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	

GEM3	MIO
USB0	MIO, USB2 only

## Constrains

### Basic module constrains

#### **\_i\_bitgen\_common.xdc**

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

### Design specific constrain

#### **\_i\_io.xdc**

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

## Software Design - Vitis

For Vitis project creation, follow instructions from:

[Vitis](#)

## Application

Template location: "<project folder>\sw\_lib\sw\_apps\"

### zynqmp\_fsbl

TE modified 2023.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te\_\*
  - Si5338 Configuration
  - ETH+OTG Reset over MIO

## zynqmp\_pmufw

Xilinx default PMU firmware.

## hello\_te0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

## u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

# Software Design - PetaLinux

---

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)

## Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
  - CONFIG\_SUBSYSTEM\_PRIMARY\_SD\_PSU\_SD\_1\_SELECT=y
- add new flash partition for bootscr and sizing
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART0\_SIZE=0xA00000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART1\_SIZE=0x2000000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART2\_SIZE=0x40000
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART3\_NAME="bootscr"
  - CONFIG\_SUBSYSTEM\_FLASH\_PSU\_QSPI\_0\_BANKLESS\_PART3\_SIZE=0x80000
- Identification
  - CONFIG\_SUBSYSTEM\_HOSTNAME="Trenz"
  - CONFIG\_SUBSYSTEM\_PRODUCT="TE0820"

## U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
  - CONFIG\_ENV\_OVERWRITE=y
  - CONFIG\_NVMEM=y
  - CONFIG\_DM\_RTC=y (needed for nvmem driver because of bug in uboot)
- Boot Modes:
  - CONFIG\_QSPI\_BOOT=y
  - CONFIG\_SD\_BOOT=y
  - CONFIG\_ENV\_IS\_IN\_FAT is not set
  - CONFIG\_ENV\_IS\_IN\_NAND is not set
  - CONFIG\_ENV\_IS\_IN\_SPI\_FLASH is not set
  - CONFIG\_BOOT\_SCRIPT\_OFFSET=0x2A40000
- Identification
  - CONFIG\_IDENT\_STRING=" TE0820"

Change platform-top.h:

```
#include <configs/xilinx_zynqmp.h> #no changes
```

## Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"

/*----- SD0 eMMC -----*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;
};

/*----- SD1 sd2.0 -----*/
&sdhci1 {
    disable-wp;
    no-1-8-v;
};

/*----- USB 2.0 only -----*/
&usb0 {
    status = "okay";
    clock-names = "bus_clk";
    clocks = <&zynqmp_clk USB0_BUS_REF>;
    assigned-clocks = <&zynqmp_clk USB0_BUS_REF>;
};

&dwc3_0 {
    dr_mode = "host";
};

/*----- ETH PHY -----*/
&gem3 {
    //required otherwise petalinux gives a static address here
    /delete-property/ local-mac-address;
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/*----- QSPI ----- */
&qspi {
```

```

#address-cells = <1>;
#size-cells = <0>;
status = "okay";
flash0: flash@0 {
    compatible = "jedec,spi-nor";
    reg = <0x0>;
    #address-cells = <1>;
    #size-cells = <1>;

    spi-rx-bus-width = <4>;
    spi-tx-bus-width = <4>;
    spi-max-frequency = <90000000>;
};

/*----- I2C -----*/
&i2c0 {
    eeprom: eeprom@50 {
        compatible = "microchip,24aa025", "atmel,24c02";
        reg = <0x50>;

        #address-cells = <1>;
        #size-cells = <1>;
        eth0_addr: eth-mac-addr@FA {
            reg = <0xFA 0x06>;
        };
    };
};

```

## Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
  - CONFIG\_CPU\_FREQ is not set

## Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- for web server app:
  - CONFIG\_busybox-httpd=y
- For additional test tools only:
  - CONFIG\_i2c-tools=y
  - CONFIG\_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- For auto login:
  - CONFIG\_imagefeature-serial-autologin-root=y

## FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"

[Petalinux Troubleshoot#Petalinux2023.2](#)

## Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps"

### startup

Script App to load init.sh from SD Card if available.

### webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

## Additional Software

---

### SI5338

File location "<project folder>\misc\SI5338\SI5338-\*.slabtimeproj"

General documentation how you work with these project will be available on [SI5338](#)

## Appx. A: Change History and Legal Notices

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### Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
<div>Error rendering macro 'page-info'  Ambiguous us method</div>	<div>Error rendering macro 'page-info'  Ambiguous us method</div>	<div>Error rendering macro 'page-info'  Ambiguous us method</div>	<ul style="list-style-type: none"><li>bugfix file_location.txt</li><li>update USB available in uboot</li></ul>



overload  
ing for  
method  
jdk.  
proxy27  
9.\$Proxy  
4022#ha  
sConten  
tLevelPe  
rmission  
.  
Cannot  
resolve  
which  
method  
to  
invoke  
for [null,  
class  
java.  
lang.  
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2024-02-23	v.78	Manuela Strücker	<ul style="list-style-type: none"> <li>• 2023.2 update</li> <li>• new assembly variants</li> </ul>
2024-02-13	v.77	Markus Kirberg	<ul style="list-style-type: none"> <li>• update Release notes and known issues</li> </ul>
2023-06-22	v.76	Manuela Strücker	<ul style="list-style-type: none"> <li>• 2022.2 update</li> <li>• new assembly variants</li> </ul>
2023-03-28	v.75	Manuela Strücker	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2022-09-28	v.74	Manuela Strücker	<ul style="list-style-type: none"> <li>• bugfix fsbl generation</li> <li>• new assembly variants</li> </ul>
2022-09-12	v.73	Manuela Strücker	<ul style="list-style-type: none"> <li>• update board part files compatible to Vivado 2021.2.1</li> <li>• new assembly variants</li> </ul>
2022-09-06	v.72	Manuela Strücker	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2022-01-26	v.70	John Hartfiel	<ul style="list-style-type: none"> <li>• add missing uboot notes</li> </ul>
2022-01-24	v.68	John Hartfiel	<ul style="list-style-type: none"> <li>• Add new delivery design with uboot bugfix</li> </ul>
2022-01-21	v.67	John Hartfiel	<ul style="list-style-type: none"> <li>• Add Known issues</li> </ul>
2022-01-14	v.66	John Hartfiel	<ul style="list-style-type: none"> <li>• 2021.2 release</li> </ul>
2021-06-09	v.65	Manuela Strücker	<ul style="list-style-type: none"> <li>• document style update</li> </ul>
2021-06-01	v.64	John Hartfiel	<ul style="list-style-type: none"> <li>• 2020.2 update</li> <li>• new assembly variants</li> <li>• document style update</li> </ul>
2020-05-07	v.62	John Hartfiel	<ul style="list-style-type: none"> <li>• update programming section</li> </ul>

2020-04-08	v.61	John Hartfiel	<ul style="list-style-type: none"> <li>• script update</li> <li>• new assembly variants</li> </ul>
2020-03-25	v.60	John Hartfiel	<ul style="list-style-type: none"> <li>• script update</li> </ul>
2020-01-21	v.59	John Hartfiel	<ul style="list-style-type: none"> <li>• Script update for linux user</li> </ul>
2020-01-14	v.58	John Hartfiel	<ul style="list-style-type: none"> <li>• Script update, new features</li> <li>• doc update</li> <li>• add missing binary files</li> </ul>
2019-12-19	v.57	John Hartfiel	<ul style="list-style-type: none"> <li>• 2019.2 release</li> </ul>
2019-10-29	v.56	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2019-08-09	v.55	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix fsbl</li> </ul>
2019-06-19	v.54	John Hartfiel	<ul style="list-style-type: none"> <li>• design changes</li> <li>• new variants</li> </ul>
2019-04-01	v.53	John Hartfiel	<ul style="list-style-type: none"> <li>• some notes</li> <li>• renamed ..D variants to ...A</li> </ul>
2018-09-21	v.47	John Hartfiel	<ul style="list-style-type: none"> <li>• 2018.3 release finished (include design reworks)</li> </ul>
2018-10-31	v.43	John Hartfiel	<ul style="list-style-type: none"> <li>• Update Design files for 2GB variants</li> <li>• rebuilt petalinux for optional init script</li> </ul>
2018-09-12	v.41	John Hartfiel	<ul style="list-style-type: none"> <li>• Update Design files for 2GB variants</li> </ul>
2018-07-11	v.40	John Hartfiel	<ul style="list-style-type: none"> <li>• add notes to ES1</li> </ul>
2018-07-06	v.38	John Hartfiel	<ul style="list-style-type: none"> <li>• 2018.2 release finished</li> </ul>
2018-06-19	v.34	John Hartfiel	<ul style="list-style-type: none"> <li>• Design Files Update</li> </ul>
2018-02-13	v.29	John Hartfiel	

			<ul style="list-style-type: none"> <li>Design Files Update</li> </ul>
2018-02-06	v.27	John Hartfiel	<ul style="list-style-type: none"> <li>Design Files Update</li> </ul>
2018-01-29	v.26	John Hartfiel	<ul style="list-style-type: none"> <li>Update Known Issues</li> </ul>
2018-01-24	v.25	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2017.4</li> </ul>
2018-01-10	v.24	John Hartfiel	<ul style="list-style-type: none"> <li>Update Known Issues</li> </ul>
2017-12-20	v.23	John Hartfiel	<ul style="list-style-type: none"> <li>Typo correction</li> <li>Update HW Module Table Description</li> </ul>
2017-11-21	v.19	John Hartfiel	<ul style="list-style-type: none"> <li>Design Update</li> </ul>
2017-11-20	v.18	John Hartfiel	<ul style="list-style-type: none"> <li>Design Update</li> <li>Add Variants with 128MB Flash</li> </ul>
2017-11-13	v.16	John Hartfiel	<ul style="list-style-type: none"> <li>Update Carrier sections</li> </ul>
2017-11-06	v.15	John Hartfiel	<ul style="list-style-type: none"> <li>Typo corrected</li> </ul>
2017-10-23	v.13	John Hartfiel	<ul style="list-style-type: none"> <li>Update Key Features section</li> <li>Style Update Additional Software section</li> </ul>
2017-10-19	v.9	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2017.2</li> </ul>
2017-09-11	v.1	<div> <div> Error renderi ng macro 'page- info'  Ambiguo us </div> </div>	Initial release

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Document change history.

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### Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

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### WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

#### Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.  
proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to  
invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due  
to overlapping prototypes between: [interface com.atlassian.confluence.user.

ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.

ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class  
com.atlassian.confluence.core.ContentEntityObject]