TE0802 TRM

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Overview

The Trenz Electronic TE0802 is a development board integrating a Xilinx Zynq UltraScale+ . Other assembly options for the FPGA and the memory chips are available. Please contact us for further information.

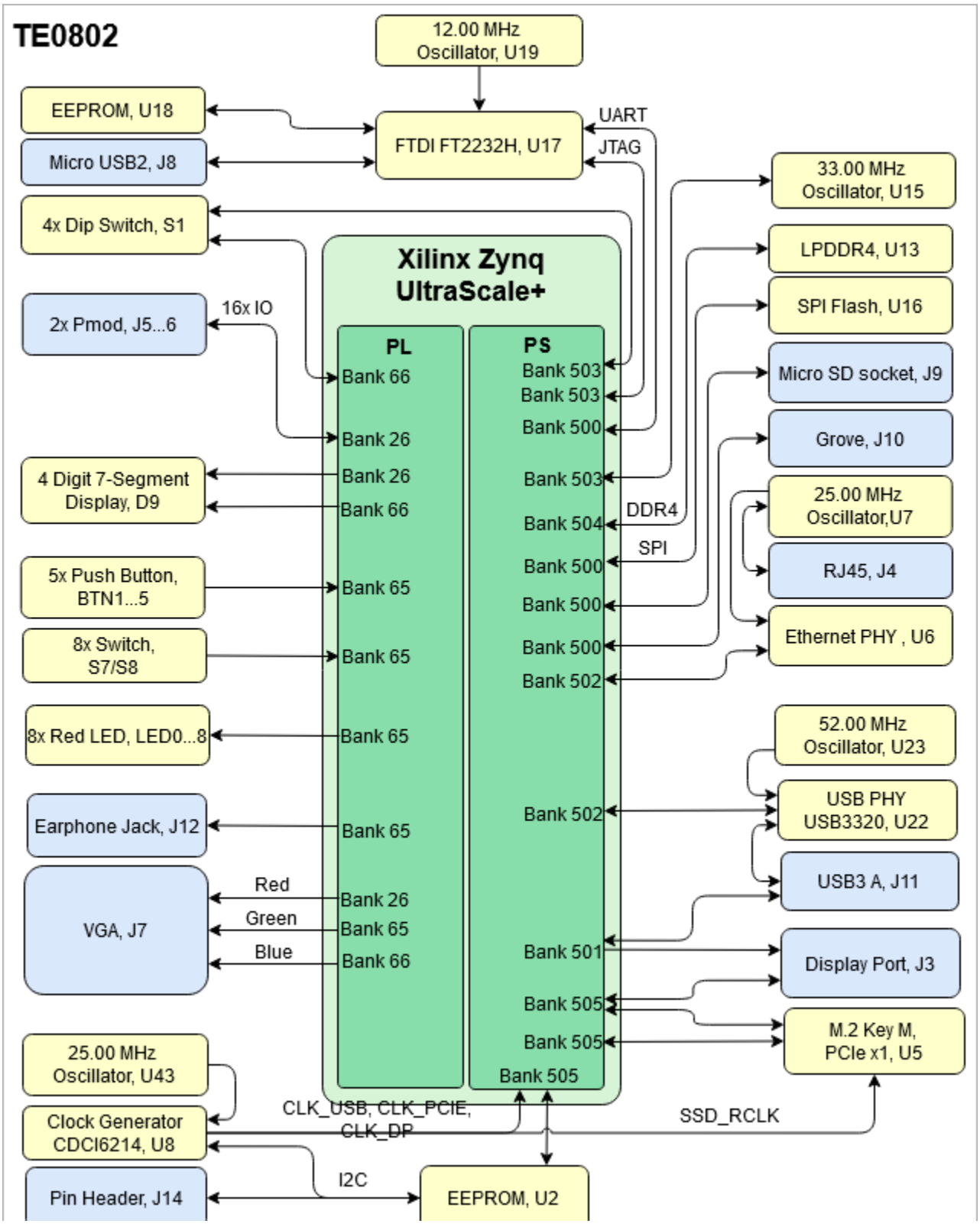
Refer to http://trenz.org/te0802-info for the current online version of this manual and other available documentation.

Key Features

- MPSoC: XCZU2CG - Xilinx Zynq UltraScale+ MPSoC
  - Package: 1SBVA484E
  - Speed Grade: -1 (Slowest)
  - Temperature Grade: Extended (0 to +100 °C)
- RAM/Storages:
  - SDRAM: LPDDR4 8Gb 256Mx16x 2
  - SPI Flash 256Mb (32M x 8) 133 MHz
  - EEPROMs 2Kb (256 x 8)
  - EEPROMs 4Kb (512 x 8)

- Interfaces:
  - USB JTAG/UART microUSB
  - 1GB Ethernet RJ45
  - USB 3.0 Host (Type A Connector)
  - microSD Card
  - M.2 SSD PCIe
  - 3.5 mm Earphone Jack (PWM Output)
  - Display Port
  - VGA
  - 4 Digit 7-Segment LED Display
  - 8 LEDs
  - 5 User Buttons
  - 8 Bit Slide Switches
  - Reset Button
  - 2x Pmod Connector
- Power
  - 5 V +/- 10%
  - ~3.5 W
- Dimension: 100mm x 100mm

Block Diagram


TE0802
12.00 MHz Oscillator, U19
EEPROM, U18
Micro USB2, J8
FTDI FT2232H, U17
UART
JTAG
4x Dip Switch, S1
33.00 MHz Oscillator, U15
LPDDR4, U13
SPI Flash, U16
Micro SD socket, J9
Grove, J10
25.00 MHz Oscillator,U7
RJ45, J4
Ethernet PHY , U6
52.00 MHz Oscillator, U23
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Xilinx Zynq UltraScale+
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Bank 65
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Bank 500
Bank 504
Bank 502
Bank 501
Bank 505
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8x Red LED, LED0...8
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CLK_USB, CLK_PCIE, CLK_DP
SSD_RCLK
Pin Header, J14
I2C
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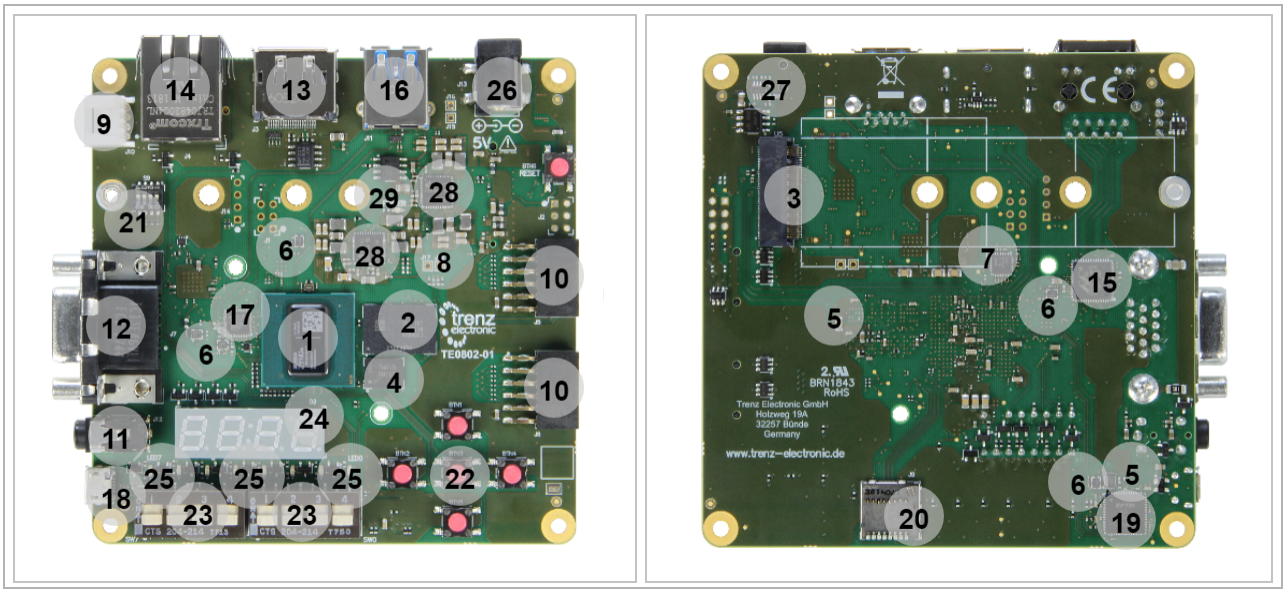
TE0802 Block Diagram

Main Components



TE0802 Main Components (Picture shows Revision 01)

1. Xilinx Zynq UltraScale+ MPSoc, U14
2. LPDDR4 SDRAM, U13
3. M.2 Key M PCIe x1, U5
4. SPI Flash Memory, U16
5. EEPROM, U2, U18
6. Oscillator, U15, U7, U19, U23, U43
7. Clock Generator, U8
8. Clock Generator Programming Connector, J14
9. Grove Connector, J10
10. Pmod Host Socket, J5...6
11. Headphone Jack, J12
12. D-Sub Connector, J7
13. DisplayPort, J3
14. RJ45 Socket, J4
15. Ethernet PHY, U6
16. USB Type A, J11
17. USB 2.0 PHY, U22
18. Micro USB 2.0 Type B, J8
19. FTDI USB 2.0 to JTAG/UART Converter, U17
20. microSD Card, J9
21. Slide Switch, S1
22. Push Button, BTN1...5
23. DIP Switch, S7...8
24. 4 Digit 7-Segment LED Display, D9
25. 8x LEDs (Red), LED0...7
26. Power Jack, J13
27. Overvoltage/Undervoltage/Reverse Supply Protector, U12
28. Power Management Integrated Circuit (PMIC), U1, U9
29. Power Good LED (Green), D12

Initial Delivery State

Storage device name	Content	Notes
SPI Flash (U16)	Not programmed	
EEPROM (U2)	Not programmed	Except Ethernet MAC
EEPROM (U18)	Programmed	FTDI Configuration
LPDDR4 SDRAM (U13)	Not programmed	

Initial Delivery State of Programmable Devices on the Module

Configuration Signals

Bootmode signals must be set through DIP Switch S1.

MODE Signal State	MODE1 S1-2(B)	MODE0 S1-1(A)	Boot Mode
MODE[2:0]=000	OFF	OFF	JTAG
MODE[2:0]=001	OFF	ON	not supported
MODE[2:0]=010	ON	OFF	QSPI(32 bit)
MODE[2:0]=011	ON	ON	SD0(2.0)

Boot Process

Reset setting is available through Push Button BTN6.

Signal	Connected to	Note
POR_B	BTN6, Push Button	Connected to nRESET

Reset Process

Signals, Interfaces and Pins

I/Os on Pin Headers and Connectors

FPGA bank number and number of I/O signals connected to the connectors:

FPGA Bank	Connector	I/O Signal Count	Voltage Level	Notes
Bank 503	Micro USB, J8 (over FTDI)	4 Single Ended	3.3 V	JTAG
Bank 500	Micro USB, J8 (over FTDI)	2 Single Ended	3.3 V	UART
Bank 500	Micro SD Card, J9	7 Single Ended	3.3 V	
Bank 502	ETH RJ45, J4 (over ETH PHY)	14 Single Ended	1.8 V	
Bank 505, 502	USB 3.0, J11 (USB2 over USB PHY)	2 Differential Pairs, 12 Single Ended	-- / 1.8V	
Bank 505, 501	SSD M.2, U5	2 Differential Pairs, 5 Single Ended	-- / 3.3 V	
Bank 505, 501	Display Port Connector, J3	2 Differential Pairs, 5 Single Ended	--/ 3.3 V	
Bank 26, 65, 66,	D-Sub Host Socket (VGA), J7	14 Single Ended	3.3 V / 1.8 V / 1.8 V	

Bank 65	Earphone, J12	3 Single Ended	1.8 V	
Bank 500	Grove Connector, J10	2 Single Ended	3.3 V	
Bank 26	Pmod Host Socket, J5	8 Single Ended	3.3 V	
Bank 26	Pmod Host Socket, J6	8 Single Ended	3.3 V	

General I/O to Pin Header and Connectors Information

Micro SD Card

TE0802 is equipped with a micro SD card connector (J9).

Schematic	Connected to	Notes
SD_DAT0	MIO 13, FPGA Bank 500	
SD_DAT1	MIO 14, FPGA Bank 500	
SD_DAT2	MIO 15, FPGA Bank 500	
SD_DAT3	MIO 16, FPGA Bank 500	
SD_CLK	MIO 22, FPGA Bank 500	
SD_CMD	MIO 21, FPGA Bank 500	
SD_CD	MIO 24, FPGA Bank 500	

Micro SD Card Connector Information

RJ45 Connector

TE0802 is equipped with a RJ45 connector and an Ethernet PHYs. RJ45 connector J4 is connected to Ethernet PHYs U6.

Pin	Schematic	ETH Pin	Notes
2	PHY_MDI0_P	MDIP[0]	
3	PHY_MDI0_N	MDIN[0]	
4	PHY_MDI1_P	MDIP[1]	
5	PHY_MDI1_N	MDIN[1]	
6	PHY_MDI2_P	MDIP[2]	
7	PHY_MDI2_N	MDIN[2]	
8	PHY_MDI3_P	MDIP[3]	
9	PHY_MDI3_N	MDIN[3]	

RJ45 Connector Information

USBs Sockets

TE0802 is equipped with a Micro USB2.0 B connector J8 and a USB3.0 connector J11.

FTDI FT2232 (U17) can be accessed through Micro USB 2.0 B connector (J8) for JTAG (channel A). Channel B is connected to the FPGA and can be used for UART.

USB2.0 Pin	Schematic	Connected to	Notes
D-	D_N	FTDI, U17	
D+	D_P	FTDI, U17	
Vbus	USB_VBUS	GND	

USB2.0 B Socket Information

USB3.0 Pin	Schematic	Connected to	Notes
D-	USB0_D_N	USB PHY, U22	
D+	USB0_D_P	USB PHY, U22	
StdA_SSRX-	USB_RX2_N	FPGA Bank 505	
StdA_SSRX+	USB_RX2_P	FPGA Bank 505	
StdA_SSTX-	USB_TX2_N	FPGA Bank 505	
StdA_SSTX+	USB_TX2_P	FPGA Bank 505	
VBUS	VBUS	USB PHY, U22	

USB3.0 A Socket Information

SSD M.2 Connector

TE0802 is equipped with a SSD M.2 connector (U5).

Pin	Schematic	Connected to	Notes
PERn0/SATA-B+	SSD_RX3_N	Pin M22, FPGA Bank 505	
PERp0/SATA-B-	SSD_RX3_P	Pin M21, FPGA Bank 505	
PERn0/SATA-A+	SSD_TXC3_N	Pin K22, FPGA Bank 505	
PERp0/SATA-A-	SSD_TXC3_P	Pin M21, FPGA Bank 505	
REFCLKN	SSD_RCLK_N	Pin 9, Clock Generator U8	
REFCLKP	SSD_RCLK_P	Pin 10, Clock Generator U8	
DAS/DSS#	SSD_DAS	MIO35, FPGA Bank 501	
DEVSLP	SSD_SLEEP	MIO32, FPGA Bank 501	
PERST#	SSD_PERSTn	MIO31, FPGA Bank 501	
CLKREQ#	SSD_CLKRQ	MIO33, FPGA Bank 501	
PEWake#	SSD_WAKE	MIO34, FPGA Bank 501	

SSD M.2 Connector Information

Display Port Connector

TE0802 is equipped with a Display Port connector (J3).

Schematic	Corresponding Signals	Connected to	Notes
DP_TX_L0_P/N	DP0_TX_P/N	Pin A19/A20, FPGA Bank 505	
DP_TX_L1_P/N	DP1_TX_P/N	Pin C19/C20, FPGA Bank 505	

DP_TX_AUX_P/N	DP_AUX_TX/RX	MIO27, MIO30, FPGA Bank 501	

Display Port Socket Information

D-Sub Connector

TE0802 is equipped with a D-Sub connector (J7).

Schematic	Corresponding Signals	Connected to	Notes
VGA_RED	VGA_R0...3	Bank 65	Red Channel
VGA_GREEN	VGA_G0...3	Bank 65	Green Channel
VGA_BLUE	VGA_B0...3	Bank 66	Blue Channel
VGA_RGB_HSYNC	VGA_HS	Bank 26	Horizontal Sync
VGA_RGB_VSYNC	VGA_VS	Bank 26	Vertical Sync

D-Sub Connector Information

Headphone Connector

TE0802 is equipped with a headphone connector (J12).

Schematic	Connected to	Notes
JACKSNS	Pin F3, FPGA Bank 65	
PWM_R	Pin F4, FPGA Bank 65	
PWM_L	Pin E3, FPGA Bank 65	

Headphone Connector Information

Grove Connector

TE0802 is equipped with a grove connector (J10).

Schematic	Connected to	Notes
Grove_SCL0	MIO18, FPGA Bank 500	
Grove_SDA0	MIO19, FPGA Bank 500	

Grove Connector Information

Pmod Sockets

TE0802 has 2 Pmod 2x6 host sockets which are connected to the FPGA.

Designator	Signals	Connected to	Notes
J5	PMOD_A0...7	Bank 26	
J6	PMOD_B0...7	Bank 26	

Pmod SMD Host Socket Information

Test Points

Test Point	Signals	Notes
TP1	+1.1V_LPDDR4	
TP2	+1.8V_MGTRAVTT	
TP3	+1.8V_PL	
TP4	FT_B_TX	
TP5	DP_TX_PWR	
TP6	GND	
TP7	GND	
TP8	PMIC2_SDA	
TP9	PMIC2_TP	
TP10	ONKEY2	
TP11	PMIC2_SCL	
TP12	DP_TX_HPD	
TP13	DP_TX_PWR	
TP14	INT_SCL1	
TP15	INT_SDA1	
TP16	FT_B_RX	
TP17	CLOCKDIST_OE	
TP18	+0.85V_VCCINT	
TP19	+3.3V	
TP20	+1.8V_PS	
TP21	ERR_STATUS	
TP22	+1.2V_PSPLL	
TP23	GND	
TP24	GND	
TP25	PMIC1_SCA	
TP26	PMIC1_SDA	
TP27	ONKEY1	
TP28	PMIC1_TP	
TP29	POR_B	
TP30	PSBATT	
TP31	SRST_B	
TP32	DONE	

TP33	INIT_B	
TP34	VBUS	
TP35	USB_VBUS	
TP36	PROG_B	
TP37	ERR_OUT	

Test Points Information

On-board Peripherals

Chip/Interface	Designator	Notes
TE0802 TRM#Quad SPI Flash Memory	U16	
TE0802 TRM#LPDDR4 SDRAM	U13	
TE0802 TRM#EEPROM	U2, U18	
TE0802 TRM#USB ULPI PHY	U22	
TE0802 TRM#Ethernet PHY	U6	
TE0802 TRM#FTDI FT2232H	U17	
TE0802 TRM#Clock Generator	U8	
Oscillators	U7, U15, U19, U23, U43	
TE0802 TRM#7-Segment Display	D9	
TE0802 TRM#User LED	LED0...7	
TE0802 TRM#Push Button	BTN1...5	
TE0802 TRM#DIP Switch	S1, S7/S.8	

On-board Peripherals

Quad SPI Flash Memory

he TE0802 evaluation board has one single QSPI flash connected as x4. Flash size depends on the assembly option, default 32MB

MIO Pin	Schematic	U16 Pin	Notes
MIO0	MIO0	B2	SPI_CLK
MIO1	MIO1	D2	SPI_DQ1
MIO2	MIO2	C4	SPI_DQ2
MIO3	MIO3	D4	SPI_DQ3
MIO4	MIO4	D3	SPI_DQ0
MIO5	MIO5	C2	SPI_CS

Quad SPI Interface MIOs and Pins

LPDDR4 SDRAM

The TE0802 evaluation board has 1 GByte volatile LPDDR4 SDRAM IC (U13) for storing user application code and data. The details depends on the assembly option.

- Part number: IS43LQ32256A-062BLI
- Supply voltage: 1.06 -1.17 V
- Speed: 1600 MHz
- Temperature: -40 to +85 C

EEPROM

MIO Pin	Schematic	U2 Pin	Notes
MIO8	Int_SCL1	SCL	
MIO9	Int_SDA1	SDA	

I2C FPGA EEPROM Interface MIOs and Pins

Type	I2C Address	Designator	Notes
4AA025E48T-I/OT	0x50	U2	EEPROM with MAC

I2C Address for FPGA EEPROM

Pin	Schematic	U18 Pin	Notes
CS	EECS	1	FTDI
CLK	EECLK	2	FTDI
DIN/DO	EEDATA	3/4	FTDI

I2C FTDI EEPROM Interface Pins

USB ULPI PHY

The TE802 is equipped with a USB ULPI PHY.

USB PHY Pin	Signal Schematic Names	Connected to	Note
DATA0	USB0_DATA0	MIO56, FPGA Bank 502	
DATA1	USB0_DATA1	MIO57, FPGA Bank 502	
DATA2	USB0_DATA2	MIO54, FPGA Bank 502	
DATA3	USB0_DATA3	MIO59, FPGA Bank 502	
DATA4	USB0_DATA4	MIO60, FPGA Bank 502	
DATA5	USB0_DATA5	MIO61, FPGA Bank 502	
DATA6	USB0_DATA6	MIO62, FPGA Bank 502	
DATA7	USB0_DATA7	MIO63, FPGA Bank 502	
DIR	USB0_DIR	MIO53, FPGA Bank 502	
NXT	USB0_NXP	MIO55, FPGA Bank 502	
STP	USB0_STP	MIO58, FPGA Bank 502	
RESETB	USB0_RST_N	MIO38, FPGA Bank 501	

CPEN	USB0_VBUS_EN	Pin 1, U21 (Current-limited Power Switch)	
VBUS	VBUS	Pin 8, U21 (Current-limited Power Switch). Pin 1, J11 (USB Connector)	
ID	USB0_ID	Pulled-down to GND	
DP	USB0_D_P	Pin 3, J11 (USB Connector)	
DM	USB0_D_N	Pin 2, J11 (USB Connector)	
REFCLK	USB0_RCLK	Pin 3, U23 (Oscillator)	
CLKOUT	USB0_CLK	MIO52, FPGA Bank 502	

USB ULPI PHY Connections and Pins

Ethernet PHY

The TE0802 is equipped with an Ethernet PHY (U6) which is connected to RJ45 (J4) connector.

Ethernet PHY Pin	Signal Schematic Names	ETH	Note
TXD0	ETH_TXD0	MIO65, FPGA Bank 502	
TXD1	ETH_TXD1	MIO66, FPGA Bank 502	
TXD2	ETH_TXD2	MIO67, FPGA Bank 502	
TXD3	ETH_TXD3	MIO68, FPGA Bank 502	
TX_CTRL	ETH_TXCTL	MIO69, FPGA Bank 502	
TX_CLK	ETH_CLK	MIO64, FPGA Bank 502	
MDIO	ETH_MDIO	MIO77, FPGA Bank 502	Pulled-up to +1.8V_PS.
MDC	ETH_MDC	MIO76, FPGA Bank 502	
MDIP[0]	PHY_MDI0_P	Pin2, J4 (RJ45)	
MDIN[0]	PHY_MDI0_N	Pin3, J4 (RJ45)	
MDIP[1]	PHY_MDI1_P	Pin4, J4 (RJ45)	
MDIN[1]	PHY_MDI1_N	Pin5, J4 (RJ45)	
MDIP[2]	PHY_MDI2_P	Pin6, J4 (RJ45)	
MDIN[2]	PHY_MDI2_N	Pin7, J4 (RJ45)	
MDIP[3]	PHY_MDI3_P	Pin8, J4 (RJ45)	
MDIN[3]	PHY_MDI3_N	Pin9, J4 (RJ45)	
LED[0]	PHY_LED0	LED, J4 (RJ45)	
LED[1]	PHY_LED1	LED, J4 (RJ45)	
CONFIG	-	-	Pulled-up to +1.8V_PS.
XTAL_IN	ETH_XTAL_IN	Pin 3, U7 (Oscillator)	
RESETn	ETH_RST	MIO37, FPGA Bank 501	Pulled-up to +1.8V_PS.
RX_CLK	ETH_RXCK	MIO70, FPGA Bank 502	
RX_CTRL	ETH_RXCTL	MIO75, FPGA Bank 502	
RXD[0]	ETH_RXD0	MIO71, FPGA Bank 502	
RXD[1]	ETH_RXD1	MIO72, FPGA Bank 502	

RXD[2]	ETH_RXD2	MIO73, FPGA Bank 502	
RXD[3]	ETH_RXD3	MIO74, FPGA Bank 502	

Ethernet PHY Connections and Pins

FTDI FT2232H

The FTDI chip U17 converts signals from USB 2.0 to a variety of standard serial and parallel interfaces. Refer to the FTDI data sheet for more information about the capacity of the FT2232H chip.
Channel A of FTDI FT2232H chip is used in MPPSE mode for JTAG. Channel B is used in UART mode.

The configuration of FTDI FT2232H chip is pre-programmed on the EEPROM U18.

FTDI Chip Pin	Signal Schematic Name	Connected to	Notes
ADBUS0	TCK	Pin H13, FPGA Bank 503	JTAG Interface
ADBUS1	TDI	Pin H12, FPGA Bank 503	JTAG Interface
ADBUS2	TDO	Pin J13, FPGA Bank 503	JTAG Interface
ADBUS3	TMS	Pin J12, FPGA Bank 503	JTAG Interface
BDBUS0	FT_B_TX	MIO10, FPGA Bank 500	UART
BDBUS1	FT_B_RX	MIO11, FPGA Bank 500	UART
EECS	EECS	Pin 1, U18 (EEPROM)	
EECLK	EECLK	Pin 2, U18 (EEPROM)	
EEDATA	EEDATA	Pin 3/4, U18 (EEPROM)	
OSCI	-	Pin 3, U19 (Oscillator)	
DM	D_N	Pin 2, J8 (Micro USB 2.0)	
DP	D_P	Pin 3, J8 (Micro USB 2.0)	

FTDI Chip Interfaces and Pins

Clock Generator

The TE0802 is equipped with a clock generator (U8).

Clock Generator Pin	Signal Schematic Names	Connected to	Note
REFP	-	Pin 3, U43 (Oscillator)	
REFSEL	REFSEL	-	Pulled-up to +3.3V.
RESETN/SYNC	CLK_GEN_RESET	Pin B5, FPGA Bank 26	Pulled-up to +3.3V.
EEPROMSEL	EEPROMSEL	-	Pulled-up to +3.3V.
SDA/GPIO2	CLK_GEN_SDA	- (Default) MIO9, FPGA Bank 500 (R185/196 required) Pin 2, J14 (Pin Header required)	Pulled-up to +3.3V. (Default) Pulled-up to +3.3V. Pulled-up to +3.3V.
SCL/GPIO3	CLK_GEN_SCL	- (Default) MIO8, FPGA Bank 500 (R185/196 required) Pin 3, J14 (Pin Header required)	Pulled-up to +3.3V. (Default) Pulled-up to +3.3V. Pulled-up to +3.3V.

OE/GPIO4	-	-	Pulled-up to +3.3V.
Y1P	CLK_Y1_P / CLK_DP_P	Pin G19, FPGA Bank 505	27 MHz
Y1N	CLK_Y1_N / CLK_DP_N	Pin G20, FPGA Bank 505	27 MHz
Y2P	CLK_Y2_P / CLK_USB_P	Pin J19, FPGA Bank 505	26 MHz
Y2N	CLK_Y2_N / CLK_USB_N	Pin J20, FPGA Bank 505	26 MHz
Y3P	CLK_Y3_P / CLK_PCIe_P	Pin L19, FPGA Bank 505	100 MHz
Y3N	CLK_Y3_N / CLK_PCIe_N	Pin L20, FPGA Bank 505	100 MHz
Y4P	CLK_Y4_P / SSD_RCLK_P	Pin 55, U5 (M.2)	100 MHz
Y4N	CLK_Y4_N / SSD_RCLK_N	Pin 53, U5 (M.2)	100 MHz

Clock Generator Connections and Pins

Clock Sources

Designator	Signal Schematic Names	Connected to	Description	Frequency	Note
U7	ETH_XTAL_IN	Pin 34, U6 (Ethernet PHY)	Clock for Ethernet	25 MHz	
U15	PS_CLK	Pin H14, FPGA Bank 503	Clock for FPGA	33 MHz	
U23	USB_CLK / USB0_RCLK	Pin 26, U22 (USB PHY)	Clock for USB	52 MHz	
U43	-	Pin 5, U8 (Clock Generator)	Clock for Clock Generator	25 MHz	

Oscillators

7-Segment Display

The TE0802 has a 4-Digit-7-Segment LED display.

Pin	Schematic	Connected to	Notes
A/L1	CA / SEG_CA	Pin E4, FPGA Bank 65	
B/L2	CB / SEG_CB	Pin D3, FPGA Bank 65	
C/L3	CC / SEG_CC	Pin N5, FPGA Bank 65	
D	CD / SEG_CD	Pin P5, FPGA Bank 65	
E	CE / SEG_CE	Pin N4, FPGA Bank 65	
F	CF / SEG_CF	Pin C3, FPGA Bank 65	
G	CG / SEG_CG	Pin R5, FPGA Bank 65	
DP	CDP / SEG_CDP	Pin N3, FPGA Bank 65	
A1	SEG_AN1	Pin A9, FPGA Bank 26	
A2	SEG_AN2	Pin B9, FPGA Bank 26	
A3	SEG_AN3	Pin A7, FPGA Bank 26	
A4	SEG_AN4	Pin B6, FPGA Bank 26	
L1-L3	SEG_AN	Pin A8, FPGA Bank 26	

7-Segment LED Pins

User LED

Schematic	Color	Connected to	Active Level	Note
LED0...7	Red	Bank 65	High	
D12	Green	U9, PMIC	High	POWER_OK

On-board LEDs

Push Button

Designator	Schematic	Connected to	Functionality	Note
BTN_1	USER_BTN_UP	Pin U2, FPGA Bank 65	User Push Button	Pulled-up to +1.8V_PL.
BTN_2	USER_BTN_LEFT	Pin R1, FPGA Bank 65	User Push Button	Pulled-up to +1.8V_PL.
BTN_3	USER_BTN_OK	Pin T1, FPGA Bank 65	User Push Button	Pulled-up to +1.8V_PL.
BTN_4	USER_BTN_RIGHT	Pin U1, FPGA Bank 65	User Push Button	Pulled-up to +1.8V_PL.
BTN_5	USER_BTN_DOWN	Pin T2, FPGA Bank 65	User Push Button	Pulled-up to +1.8V_PL.
BTN_6	POR_B	Pin 38, U1 (PMIC), Pin 38, U9 (PMIC), Pin K12, FPGA Bank 503	Reset Button	Pulled-up to +3.3V.

On-board Push Buttons

DIP Switch

Designator	Schematic	Connected to	Functionality	Note
S1-1(A)	MODE0	Pin J16, FPGA Bank 503	DIP	Pulled-down to GND.
S1-2(B)	MODE1	Pin H15, FPGA Bank 503	DIP	Pulled-down to GND.
S1-3(C)	USER_CFG0	Pin A4, FPGA Bank 66	DIP	Pulled-down to GND.
S1-4(D)	USER_CFG1	Pin B4, FPGA Bank 66	DIP	Pulled-down to GND.
S7-1(A)	USER_SW7	Pin M5, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S7-2(B)	USER_SW6	Pin M4, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S7-3(C)	USER_SW5	Pin J2, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S7-4(D)	USER_SW4	Pin K1, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S8-1(A)	USER_SW3	Pin L1, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S8-2(B)	USER_SW2	Pin M1, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S8-3(C)	USER_SW1	Pin P2, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.
S8-4(D)	USER_SW0	Pin P3, FPGA Bank 65	DIP	Pulled-up to +1.8V_PL.

DIP Switches

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 3 A for system startup is recommended.

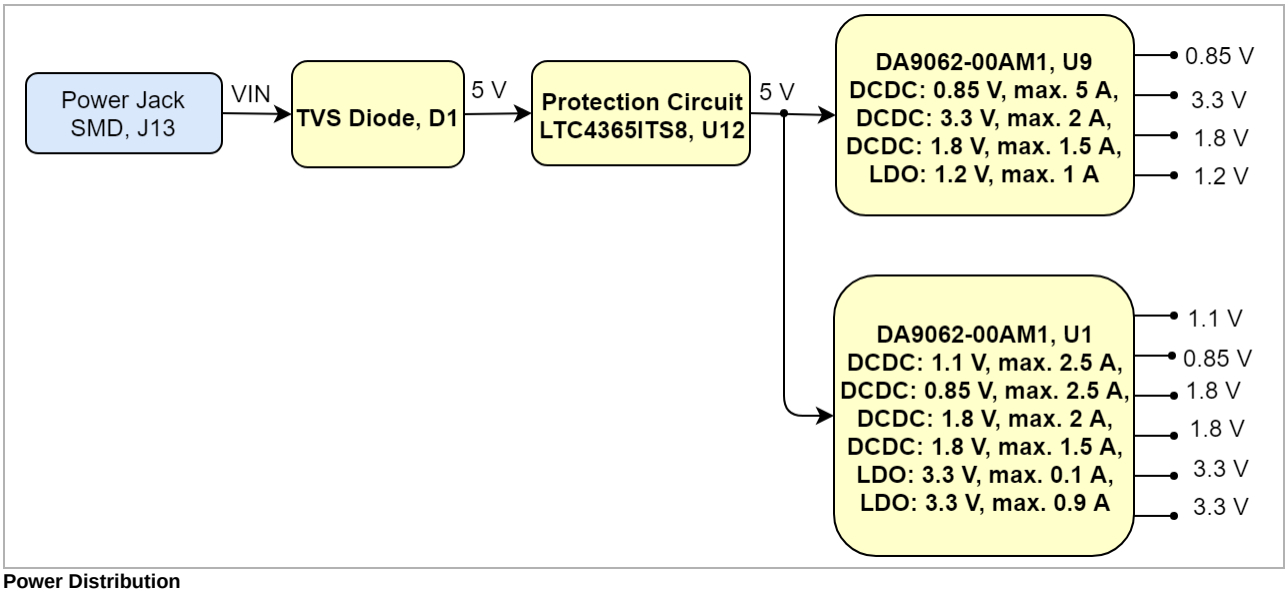
Power Consumption

Power Input Pin	Typical Current
VIN	TBD*

Power Consumption

* TBD - To Be Determined

Power Distribution Dependencies



Power Distribution

Power-On Sequence

PMICs will be reset after pressing Push Button BTN6 (POR_B).

Power Rails

Power Rail Name	Direction	Notes
VIN	IN	Supply Voltage
+5V	Out	J1...2
+3.3V	Out	J14, J10

Module Power Rails

Bank Voltages

Bank	Schematic Name	Voltage	Notes
Bank 26	+3.3V	3.3 V	

Bank 65	+1.8V_PL	1.8 V	
Bank 66	+1.8V_PL	1.8 V	
Bank 500	+3.3V	3.3 V	
Bank 501	+3.3V	3.3 V	
Bank 502	+1.8V_PS	1.8 V	
Bank 503	+3.3V	3.3 V	
Bank 504	+1.1V_LPDDR4	1.1 V	
Bank 505	+0.85V_MGTRAVCC	0.85 V	

SoC Bank Voltages

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
VIN	Input Supply Voltage (J13)	-3.5	7	V
T_STG	Storage Temperature	-40	85	°C

Absolute Maximum Ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

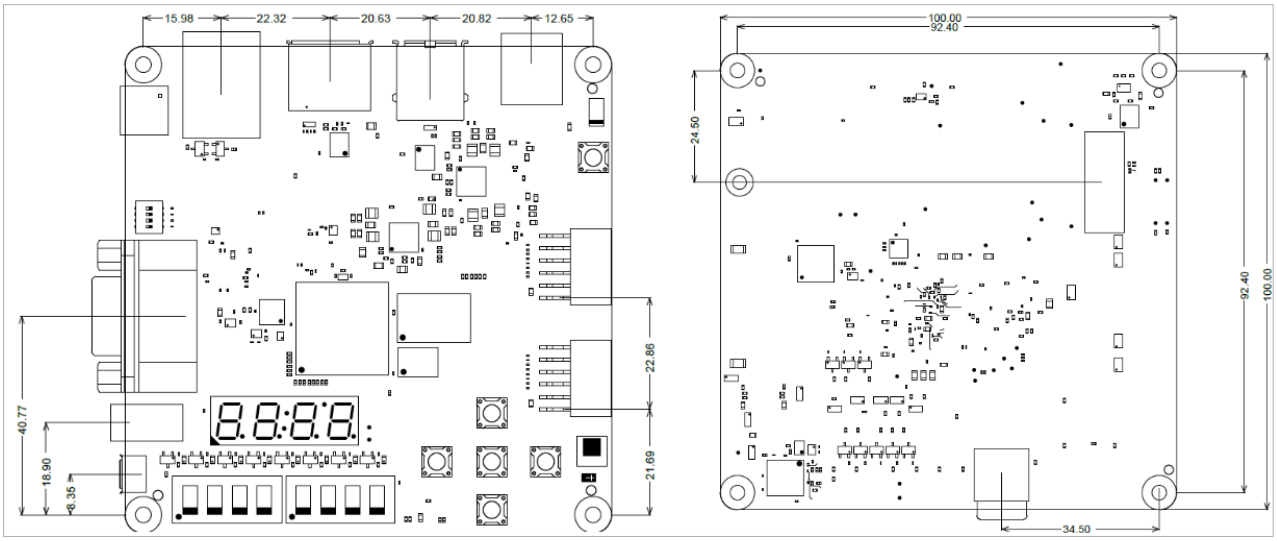
Parameter	Min	Max	Units	Reference Document
VIN	4	5.5	V	Schematic "POWER" (Component: LTC4365ITS8)
T_STG	0	85	°C	Zynq Ultrascale+ Data sheet

Recommended Operating Conditions

Physical Dimensions

Module size: 100 mm × 100 mm. Please download the assembly diagram for exact numbers.

PCB thickness: 1.48 mm



Physical Dimension in mm

Currently Offered Variants

Trenz Shop TE0802 Overview Page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-04-29	02	• Added suppressor 1SMA5.0AT3G on power input • Changed OV and UV protection range • Changed VGA schematic • USB page: VBUS resistor changed on 1K	REV02
2018-10-17	01	Release	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Board Hardware Revision Number

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Typo correction
2020-11-19	v.65	Pedram Babakhani	• initial release

--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• --

Document Change History

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

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