TEF1002 Getting Started

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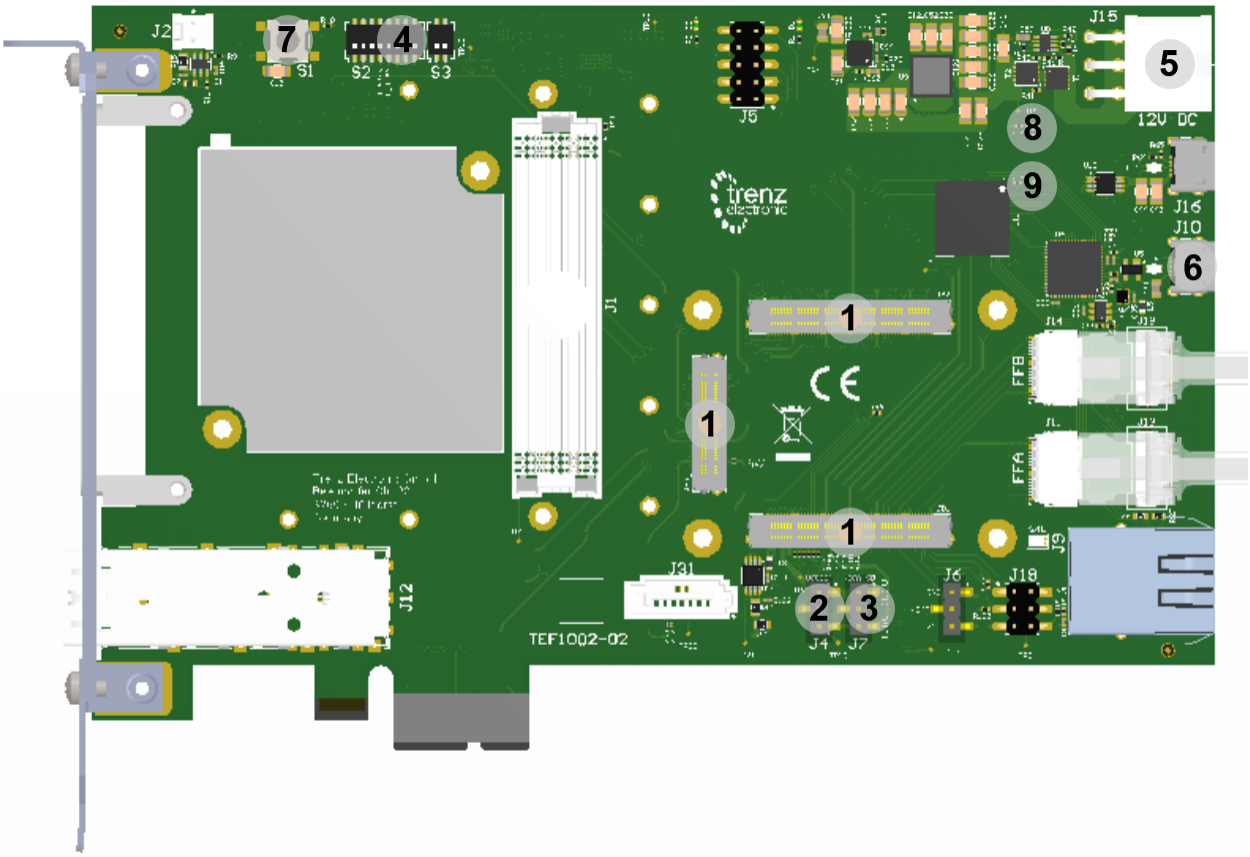
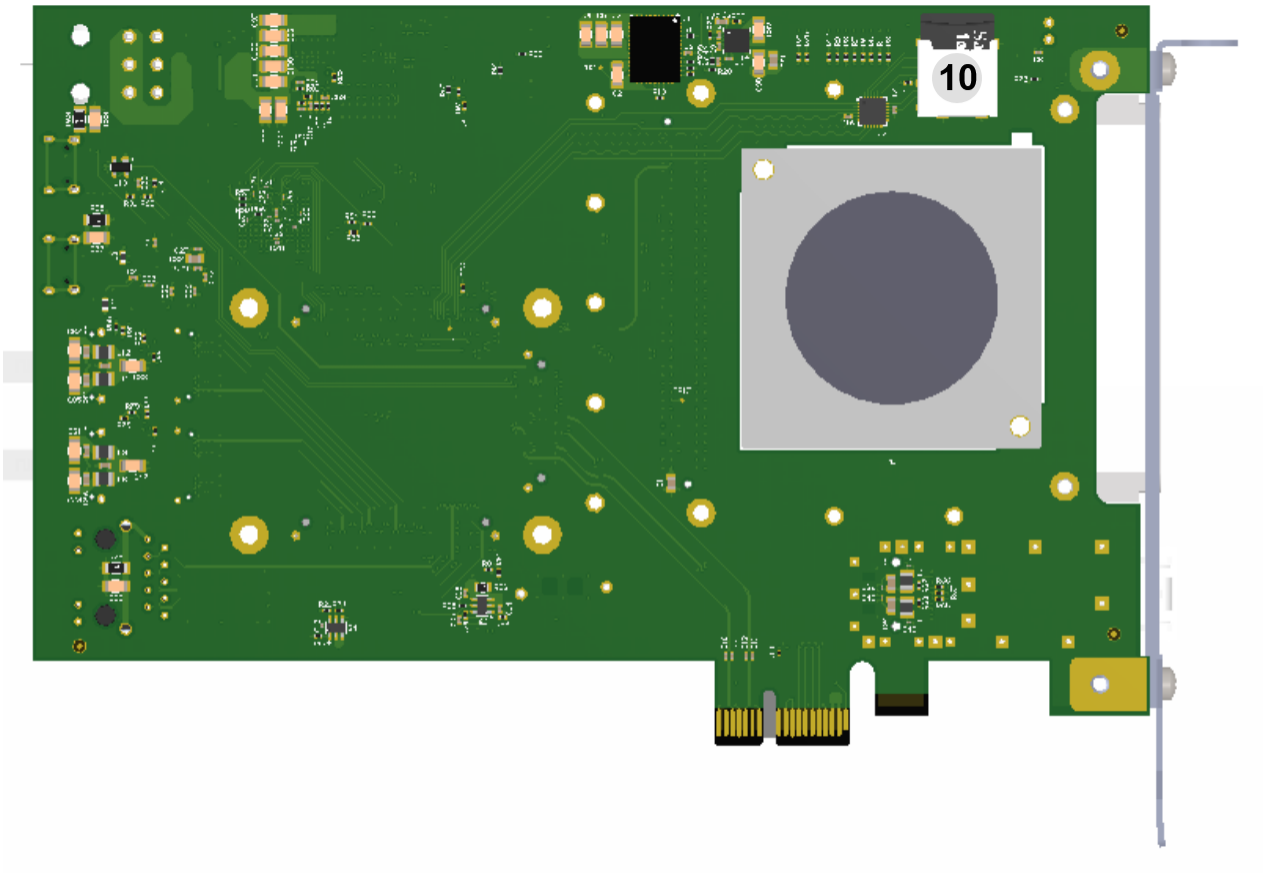
TEF1002

Overview





Board Overview

1. 4x5 module connectors
2. Jumper J4 (VCCIOA)
3. Jumper J7 (VCCA_SD)
4. Dip switches S2 and S3
5. 6-pin PCIe ATX Power Connector
6. micro USB connector for FTDI USB to JTAG/UART bridge
7. Reset push button
8. Power LED
9. Status LED
10. microSD card cage

Power supply

Single 12V power supply with minimum current capability of 3A is recommended to power on the board via the 6-pin PCIe ATX connector.

DIP-Switches and Push Buttons

Select dip switch settings according to the attached 4x5 module and your needs. Compare setting with TRM of your module and table in TRM of TEF1002. Following a general configuration is shown.

Dip	Setting	Note
S1		Push button configured by CPLD as reset

S2-1	OFF	The choice OFF, ON, OFF selects 1.8V FMC_VADJ, which is a valid bank power for TE0720.
S2-2	ON	
S2-3	OFF	
S2-4	OFF	Selects 4x5 module SOC/FPGA JTAG
S2-5	OFF	
S2-6	OFF	
S2-7	ON	Module power enable.
S2-8	OFF	Extended power sequenzing (if implemented).
S3-1	OFF	For Zynq modules: Primary Boot Mode SD/QSPI. OFF corresponds to boot from SD card.
S3-2	OFF	Overide automatic enable FMC_VADJ. (1)(2)

DIP Switches /Push Buttons

(1) Set to ON for TE0720 because bank 34 has to be powered to start up. Therefore FMC VADJ has to be set to a valid value e.g. 1.8V (See S2-1 to S2-3).

(2) For TE0820 set to on to use CLK0 (VCCO 65). Therefore FMC VADJ has to be set to a valid value e.g. 1.8V (See S2-1 to S2-3).

Jumpers

For Jumper J7 compare TRM of actually used 4x5 module. The voltage of the bank where the SDIO signals reside has to selected. J4 selects the module bank voltage VCCIOA. It has to be selected in accordance with IO voltage of signals connected to FFA and FFB. If both FFA and FFB are not used any setting is ok. Do not leave open (communication of 4x5 module with TEF1002 CPLD is only possible with availabe VCCIOA)!

Jumper	Power Rail	3.3V	1.8V	Remark
J7	VCCA_SD	1-2	2-3	Powers SDIO Levelshifter on 4x5 module side.
J4	VCCIOA	1-2	2-3	Powers 4x5 bank, where FFA and FFB high speed signals are connected.

Jumpers

LEDs

There are four LEDs on the board. Two of them are user LEDS not further described here. Compare corresponding table in TEF1002 TRM.

LED	Connected to	Function	Notes
D3	3V3IN	Power	ON when 3.3V generated from 12V input is up
D4	SC CPLD U11, Pin C2	Status	SC CPLD firmware dependent, for further description see firmware description.

Carrier LEDs

JTAG/UART

JTAG (first FTDI port) and UART (second FTDI port) is available via MicroUSB. External JTAG Programmer is not needed.

Reference Designs

- Use the Test board Reference Design of the installed 4x5 module.
- For TE0820 on this carrier TE0820 TD TEF1002, including PCIe endpoint and SATA, is available.

Notes

- TEF1002 Resources