Project Delivery - Intel devices

Table of contents

- 1 Quick Start
- 2 Zip Project Delivery
  - 2.1 Zip Project Delivery
  - 2.2 Main Supported Release
    - 2.2.1 Currently limitations of functionality
  - 2.3 Directory structure
  - 2.4 Command Files
    - 2.4.1 Create_project_win.cmd/_create_project_linux.sh
- 3 Design Environment - Usage
  - 3.1 Reference Design - Getting Started
  - 3.2 Hardware Design
    - 3.2.1 Device list CSV Description
  - 3.3 Advanced Usage
    - 3.3.1 User defined device list csv file
    - 3.3.2 User defined Settings
- 4 Checklist / Troubleshoot
- 5 References
- 6 Document Change History
- 7 Table of contents

Quick Start

The most Trenz Electronic FPGA Reference Designs are TCL-script based projects.

The "normal" Quartus project will be generated in the subfolder "/quartus/" and the additional software part will be generated in the subfolder "/software/" after executing scripts.

To create project do the following steps:

1. Execute "create_project_win.cmd" or "create_project_linux.sh"
2. Select your board in "Board selection"
3. Click on "Create project" button

For more details and manual configuration of design basic settings, see Reference Design - Getting Started.

For Problems, please check Checklist / Troubleshoot at first.

Zip Project Delivery

Zip Name Description

Description	PCB Name		Project Name+ (opt. Variant)		supported	Quartus Version	Date	
Example:	TEI0006	-	test_board (_noprebuilt)	-	quartus_22.4	-	20230918161807	.zip

Last supported Release

Type or File	Version	Note
Quartus Prime	22.1 Lite / 22.4 Pro	--
Trenz Project Scripts	22.0	--
Trenz <board_series>_devices.csv	1.1	--
Trenz zip_ignore_list.csv	1.2	--
Trenz zip.teinfo	1.0	--
Trenz mod_list.csv	1.3	--
Trenz apps_list.csv	1.1	--
Trenz prod_cfg_list.csv	1.1	internal usage only

Currently limitations of functionality

- Quartus Prime Lite 19.1 for Windows: requires a patch
  - Reason: error message when generating any EMIF IP or Cyclone® V /Arria® V HPS IP
  - Workaround: See https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/tools/2020/fatal--cannot-generate-ip-in-a-windows-evironment-.html
- Quartus Prime Lite 20.1.1 for Windows:
  - Reason: Error: (11133): IP component with file "<path to file>" upgrade failed
  - Workaround: Add "<ALIAS>GPIO Lite Intel FPGA IP v20.1</ALIAS>" to *.lst file in Quartus installation directory: e.g. C:\intelFPGA_lite\20.1\ip\altera\altera_gpio_lite\altera_gpio_lite_wizard.lst
- Quartus Prime Lite 21.1 for Windows:
  - Reason: Error: (11133): IP component with file "<path to file>" upgrade failed
  - Workaround: Add "<ALIAS>GPIO Lite Intel FPGA IP v21.1</ALIAS>" to altera_gpio_lite_wizard.lst file in Quartus installation directory: C:\intelFPGA_lite\21.1\ip\altera\altera_gpio_lite\altera_gpio_lite_wizard.lst

Directory structure

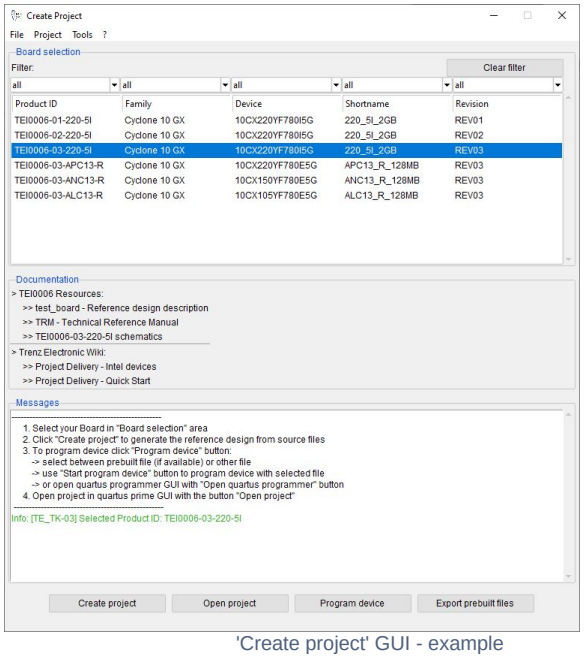
File or Directory	Type	Description
<project folder>	work, base directory	Base directory with predefined batch files (*.cmd, *.sh) to create quartus project, open quartus project or program device
<project folder>/backup/	generated	(Optional) Directory for project backups
<project folder>/_binaries_<articlenumber>	generated	export directory for binaries (run create_project_win.cmd (Win OS) / create_project_linux.sh (Linux OS)" and select "Export prebuilt files" button)
<project folder>/board_files/	source	Local list of available board variants (<board_series>_devices.csv)
<project folder>/log/	generated	(Temporary) Directory with quartus log files (used only with predefined commands from tcl scripts, otherwise this logs will be writen into the quartus work directory)
<project folder>/prebuilt/	prebuilt	Contains subfolders for different board variants
<project folder>/prebuilt/<board_part_shortname>	prebuilt	Directory with prebuilt programming files (*.pof, *.sof or *.jic, *.rbf) for FPGA and different source files for hardware (*.sopcinfo) and software (*.elf) included in subfolders

<project folder>/prebuilt/<board_part_shortname>/programming_files/	prebuilt	Directory with prebuilt programming files (*.pof, *.sof or *.jic, *.rbf)
<project folder>/prebuilt/<board_part_shortname>/hardware/	prebuilt	Directory with prebuilt hardware sources (*.sopcinfo)
<project folder>/prebuilt/<board_part_shortname>/software/	prebuilt	(Optional) Directory with prebuilt software sources (*.elf)
<project folder>/prebuilt/<board_part_shortname>/os/	prebuilt	(Optional) Directory with predefined OS images included in subfolders
<project folder>/quartus/	generated	(Temporary) Directory where quartus project is created. Quartus project file is <project_name>.qpf
<project folder>/scripts/	source	TCL scripts to build a project
<project folder>/settings/	source	(Optional) Additional design settings: zip_ignore_list.csv, mod_list.csv, design_basic_settings.tcl, zip.teinfo
<project folder>/software/	generated	(Temporary) Directory with additional software project
<project folder>/os/	generated	(Temporary) Directory with additional OS files in subfolders
<project folder>/source_files/	source	Directory with source files needed for create project
<project folder>/source_files/quartus/ <project folder>/source_files/<Board Part Shortname>/quartus	source	Source files for quartus project (Optional) Source files for specific assembly variants
<project folder>/source_files/software/ <project folder>/source_files/<Board Part Shortname>/software	source	(Optional) Source files for additional software (Optional) Source files for specific assembly variants
<project folder>/source_files/os/	source	(Optional) Directory with additional os sources in in subfolders "<os_name>"

Command Files

create_project_win.cmd/create_project_linux.sh

Use to create project, open project or program device.



'Create project' GUI - example

- **Board selection**

  Select your board from listed modules. To find easier the correct board you can use the filter function. Click on "Clear filter" button to reset the filter and show all available modules.

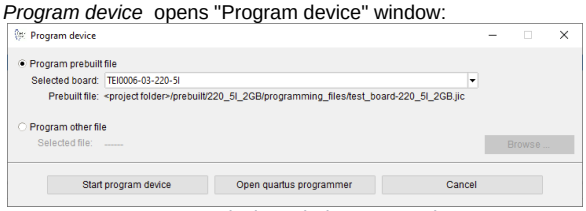
- **Documentation**

  Some links to more information about the board, reference design, schematics and create_project_win.cmd/create_project_linux.sh gui.

- **Messages**

  Messagebox shows different info, warning and error messages.

- **Buttons**
  1. *Create project* start create project from source files for selected board in "Board selection".
  2. *Open project* open existing project in quartus prime gui.
  3. *Program device* opens "Program device" window:



'Program device' window - example

- Select between "Program prebuilt file" (if available, download reference design with prebuilt files is required) and "Program other file" (select your own generated file via "Browse ..." button).
- Buttons:
  - *Browse ...* choose path to own generated programming file
  - *Start program device* start program device with selected programming file
  - *Open quartus programmer* open Quartus Programmer GUI
  - *Cancel* Quit "Program device" window

4. *Export prebuilt files* export prebuilt files for the selected board to "<project folder>/_binaries_<articlenumber>/"

Design Environment - Usage

Reference Design - Getting Started

- Install "Quartus Prime Lite Edition Version 22.1" or "Quartus Prime Pro Edition Version 22.4" (depending on used FPGA) as described in Install Intel Development Tools
- WinOS: for a reference design with Nios II install WSL1 as described in Install Intel Development Tools#NiosIIEDS-Windows
- For a reference design with Nios V install RiscFree IDE for Intel® FPGAs as described here:
  - Windows: Install Intel Development Tools#RiscFreeIDEforIntelFPGAs-Windows
  - Linux: Install Intel Development Tools#RiscFreeIDEforIntelFPGAs-Linux

Create project:

1. Run "create_project_win.cmd" or "create_project_linux.sh"
   - "<project folder>/settings/desgin_basic_settings.tcl" will be configured automatically
2. select your Board in "Board selection" section
3. click on "Create project" to generate project for selected board

Manual configuration of the design basic settings:

> Attention: Scripts are supported only with predefined quartus version!

- Open “<project folder>/settings/design_basic_settings.tcl” with a text editor:
  Set correct quartus environment:
  Example for quartus lite edition:
  QUARTUS_PATH_WIN=C:/intelFPGA_lite (quartus installation path for Win OS)
  QUARTUS_PATH_LINUX=~/intelFPGA_lite (quartus installation path for Linux OS)
  QUARTUS_VERSION=22.1std
  QUARTUS_EDITION=Lite
  Example for quartus pro edition:
  QUARTUS_PATH_WIN=C:/intelFPGA_pro (quartus installation path for Win OS)
  QUARTUS_PATH_LINUX=~/intelFPGA_pro (quartus installation path for Linux OS)
  QUARTUS_VERSION=22.4
  QUARTUS_EDITION=Pro
  Software settings are searched in (e.g. for Win OS):
  %QUARTUS_PATH_WIN%/%QUARTUS_VERSION%/quartus/
  %QUARTUS_PATH_WIN%/%QUARTUS_VERSION%/nios2eds/
  %QUARTUS_PATH_WIN%/%QUARTUS_VERSION%/niosv/
  Example directory: C:/intelFPGA_pro/22.4/

Programming FPGA or flash memory:

- General steps:
  1. Connect your Hardware-Modul to the PC via JTAG
  2. Open create_project_win.cmd/create_project_linux.sh
  3. Select correct board in "Board selection"
  4. Click on "Program device" button The "Program device" window opens.
- Program with prebuilt files: (download reference design with prebuilt files is required)
  4. Select "Program prebuilt file"
  5. Click on "Start program device" button
- Program with own generated files:
  6. Select "Program other file"
  7. Click on "Browse ..." to choose path to your own generated file (supported file types: *.jic, *.

pof, *.sof)
8. Click on "Start program device" button

- Program device via Quartus Programmer:
  9. Click on "Open quartus programmer"
  10. Select from Programmer top menu: Edit Hardware Setup, select "Arrow-USB-Blaster *" and close window
  11. Click on "Add File..." and choose correct programming file
  12. Enable "Program/Configure" checkbox and click on "Start" to program the device with the selected programming file

Hardware Design

Device list CSV Description

Device list csv file is used for TE-Scripts only.

Name	Description	Value
ID	ID to identify the board variant of the module series, used in TE-Scripts	Number, should be unique in csv list
PRODID	Product ID	Product Name
FAMILY	FPGA family, used in Quartus and TE-Scripts	device family, which is available in Quartus, ex. MAX 10
DEVICE	FPGA device, used in Quartus and TE-Scripts	device, which is available in Quartus, ex. 10M08SAU169C8G
SHORTNAME	Subdirectory name, used for multi board projects to get correct sources and save prebuilt data	name to save prebuilt files or search for sources
FLASHTYP	Flash typ used for programming Devices via Quartus/LabTools	"<Flash Name from Quartus>|<SPI Interface>" or "NA" , NA is not defined
FLASH_SIZE	Size of Module Flash	use MB, for ex. "64MB" or "NA" if not available
DDR_DEV	DDR Module	DDR module name
DDR_SIZE	Size of Module DDR	use GB or MB, for ex. "2GB" or "512MB" or "NA" if not available
PCB_REV	Supported PCB Revision	"<supported PCB Revision>|<supported PCB Revision>", for ex. "REV02" or "REV03|REV02"
NOTES	Additional notes	

Advanced Usage

Attention not all features of the TE-Scripts are supported in the advanced usage!

User defined device list csv file

To modifiy current device csv list, make a copy of the original csv and rename with suffix "_mod.csv", ex. TEI0006_devices.csv as TEI0006_devices_mod.csv. Scripts use modified csv instead of the original file.

User defined Settings

- ZIP ignore list:
  - Files which should not be added in the backup file can be defined in this file: "<project folder>/settings/zip_ignore_list.csv". This file will be loaded automatically on script initialisation.
- mod list:
  - List with commands to modify source files during project creation (<project folder> /settings/mod_list.csv).
- apps list:
  - List with software projects assigned to the correct quartus project and *.sopcinfo file (<project folder>/source_files/software/apps_list.csv).
- Qsys preset files:
  - Predefined settings for Qsys IP Components (<project folder>/source_files/quartus/ip /presets/*.qprs). They will be copied to <project folder>/quartus/ip/presets folder on project creation.

Checklist / Troubleshoot

1. Are you using exactly the same Quartus version? If not then the scripts will not work, no need to try.
2. Are you using Quartus on Windows PC? Quartus works in Linux also, but the scripts are tested on Windows only.
3. Win OS only: Use short path name, OS allows only 256 characters in normal path.
4. Linux OS only: Use bash as shell and add access rights to bash files. Check with "ls /bin/sh". It should be display: /bin/sh -> bash. Access rights can be changed with "chmod"
5. Are space character on the project path? Somtimes TCL-Scripts can't handle this correctly. Remove spaces from project path.
6. Did you have the newest reference design build version? Maybe it's only a bug from a older version.
7. On project creation process old files will be deleted. Sometimes the access will be denied by os (synchronisiation problem) and the scripts canceled. Please try again.
8. If nothing helps, send a mail to Trenz Electronic Support (support[at]trenz-electronic.de) with subject line "[TE-Reference Designs] ", the complete zip-name from your reference design.

References

1. Intel Quartus Prime User Guide: Getting Started (UG-20129)
2. Intel Quartus Prime User Guide: Platform Designer (UG-20130)
3. Intel Quartus Prime User Guide: Design Compilation (UG-20132)
4. Intel Quartus Prime User Guide: Scripting (UG-20144)

Document Change History

To get content of older revision got to "Change History" of this page and select older revision number.

Date	Revision	Quartus Version	Authors	Description
		22.1 Lite 22.4 Pro		• update to Quartus Version 22.1 Lite and 22.4 Pro

Error rendering macro 'page-info'	**Error rendering macro 'page-info'**		**Error rendering macro 'page-info'**
Am	Am		Am
big	big		big
uou	uou		uou
s	s		s
met	met		met
hod	hod		hod
ove	ove		ove
rloa	rloa		rloa
din	din		din
g	g		g
for	for		for
met	met		met
hod	hod		hod
jdk.	jdk.		jdk.
pro	pro		pro
xy2	xy2		xy2
41.	41.		41.
$Pr	$Pr		$Pr
oxy	oxy		oxy
349	349		349
6#h	6#h		6#h
asC	asC		asC
ont	ont		ont
ent	ent		ent
Lev	Lev		Lev
elP	elP		elP
erm	erm		erm
issi	issi		issi

on.
Ca
nno
t
res
olv
e
whi
ch
met
hod
to
inv
oke
for
[nul
l,
clas
s
jav
a.
lan
g.
Stri
ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
pag
es.
Pag

on.
Ca
nno
t
res
olv
e
whi
ch
met
hod
to
inv
oke
for
[nul
l,
clas
s
jav
a.
lan
g.
Stri
ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
pag
es.
Pag

on.
Ca
nno
t
res
olv
e
whi
ch
met
hod
to
inv
oke
for
[nul
l,
clas
s
jav
a.
lan
g.
Stri
ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
pag
es.
Pag

e]
due
to
ove
rlap
pin
g
prot
oty
pes
bet
we
en:
[int
erfa
ce
co
m.
atla
ssia
n.
con
flue
nce
.
use
r.
Co
nflu
enc
eUs
er,
clas
s
jav
a.
lan
g.
Stri

e]
due
to
ove
rlap
pin
g
prot
oty
pes
bet
we
en:
[int
erfa
ce
co
m.
atla
ssia
n.
con
flue
nce
.
use
r.
Co
nflu
enc
eUs
er,
clas
s
jav
a.
lan
g.
Stri

e]
due
to
ove
rlap
pin
g
prot
oty
pes
bet
we
en:
[int
erfa
ce
co
m.
atla
ssia
n.
con
flue
nce
.
use
r.
Co
nflu
enc
eUs
er,
clas
s
jav
a.
lan
g.
Stri

ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
cor
e.
Co
nte
ntE
ntit
yO
bje
ct]
[int
erfa
ce
co
m.
atla
ssia
n.
use
r.
Use
r,
clas
s
jav
a.
lan
g.

ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
cor
e.
Co
nte
ntE
ntit
yO
bje
ct]
[int
erfa
ce
co
m.
atla
ssia
n.
use
r.
Use
r,
clas
s
jav
a.
lan
g.

ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
cor
e.
Co
nte
ntE
ntit
yO
bje
ct]
[int
erfa
ce
co
m.
atla
ssia
n.
use
r.
Use
r,
clas
s
jav
a.
lan
g.

Stri ng, clas s co m. atla ssia n. con flue nce . cor e. Co nte ntE ntit yO bje ct]	Stri ng, clas s co m. atla ssia n. con flue nce . cor e. Co nte ntE ntit yO bje ct]		Stri ng, clas s co m. atla ssia n. con flue nce . cor e. Co nte ntE ntit yO bje ct]	
2022-06-27	v.14	21.1 Lite 21.4 Pro	Thomas Dück	• update to Quartus Version 21.1 Lite and 21.4 Pro
2021-06-17	v.11	20.1 Lite 20.4 Pro	Thomas Dück	• update to Quartus Version 20.1.1 lite and 20.4 pro
2020-05-13	v.9	19.1 Lite 19.4 Pro	Thomas Dück	• update to Quartus Version 19.1 lite and 19.4 pro • changed to tcl/tk
2019-11-11	v.5	18.1	Thomas Dück	• add description for *.sh files (Linux OS)
2019-10-29	v.4	18.1	Thomas Dück	• initial release
	All			

Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPerm

issi
on.
Ca
nno
t
res
olv
e
whi
ch
met
hod
to
inv
oke
for
[nul
l,
clas
s
jav
a.
lan
g.
Stri
ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
pag
es.

Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.

Stri
ng,
clas
s
co
m.
atla
ssia
n.
con
flue
nce
.
cor
e.
Co
nte
ntE
ntit
yO
bje
ct]
[int
erfa
ce
co
m.
atla
ssia
n.
use
r.
Use
r,
clas
s
jav
a.
lan

			g. Stri ng, clas s co m. atla ssia n. con flue nce . cor e. Co nte ntE ntit yO bje ct]	