

TEF1002 SC CPLD MAX10

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Overview

TEF1002 SC CPLD design for MAX10 with designator U11: 10M08SAU169C8G.

Feature Summary

- Power Management
 - SATA pin 7 power control
- Status LED
- FMC VADJ Power
- SFP control
- FFA & FFB control
- JTAG MUX
- Module control
- RESET
- I²C MUX
- PHY LEDs
- RGPIO
- USR LED

Firmware Revision and supported PCB Revision

See Document Change History.

Product Specification

Port Description

VHDL Port name	Direction	SC CPLD Pin	Connected to	Function	Notes
ACBUS0		A4	FTDI U4, pin 22	GPIO's available to user	currently not used/implemented (FIFO or other FTDI functions when FTDI reprogrammed)
ACBUS1		B4	FTDI U4, pin 23		
ACBUS2		A5	FTDI U4, pin 24		
ACBUS3		B5	FTDI U4, pin 25		
ACBUS4		A6	FTDI U4, pin 26		
ACBUS5		B6	FTDI U4, pin 27		
ACBUS6		A7	FTDI U4, pin 28		
ACBUS7		A8	FTDI U4, pin 29		
ADBUS4		A2	FTDI U4, pin 17		
ADBUS5		B2	FTDI U4, pin 18		
ADBUS6		A3	FTDI U4, pin 19		
ADBUS7		B3	FTDI U4, pin 20		
P_TCK	IN	G2	J5, pin 1	JTAG signals from pin header J5 for SC CPLD programming (S2-4 ON)	Can be used as additional IOs via JTAG pinsharing, JTAGEN (S2-4 OFF). Schematic signal names without 'P_'.
P_TDI	IN	F5	J5, pin 9		
P_TDO	OUT	F6	J5, pin 3		
P_TMS	IN	G1	J5, pin 5		
F_TCK	IN	H2	FTDI U4, pin 12	Forwarded JTAG signals from FTDI chip. Signal names: TCK, TDI, TDO, TMS	(FIFO or other FTDI functions when FTDI reprogrammed)
F_TDI	IN	G4	FTDI U4, pin 13		
F_TDO	OUT	F4	FTDI U4, pin 14		
F_TMS	IN	H5	FTDI U4, pin 15		
M_TCK	OUT	H5	JB2, pin 100	4x5 Module JTAG	Bank with VCCIO is VREF_JTAG from Module
M_TDI	OUT	J2	JB2, pin 96		
M_TDO	IN	J1	JB2, pin 98		
M_TMS	OUT	H6	JB2, pin 94		
FMC_TCK	OUT	F8	J1, pin D29	FMC JTAG	TRST not used
FMC_TDI	OUT	M7	J1, pin D30		
FMC_TDO	IN	N7	J1, pin D31		
FMC_TMS	OUT	M8	J1, pin D33		
FMC_TRST		N8	J1, pin D34		
PCIE_TCK		L11	J3, pin A5	PCIe JTAG	Currently not used
PCIE_TDI		N12	J3, pin A6		
PCIE_TDO		M12	J3, pin A7		

PCIE_TMS		M13	J3, pin A8		
PCIE_TRST		G10	J3, pin B9		
PCIE_PERST	IN	F12	J3, pin A11	Indication that PCIe Bus is up (power, clocks)	
EN_FMC	OUT	L4	U14, pin 9	Enable switched 3.3V FMC power	pulled down
EN_FMC_VADJ	OUT	K7	U1, pin 41	Enable IO power FMC_VADJ	pulled down
EN_PER	OUT	F13	Q4, pin 5	Enable periphery power 3V3_PER	pulled down
FAN_FMC_EN	OUT	K8	Q1, pin 5	Enable FMC FAN	floating during configuration (no pull down)
FMC_PG_C2M	OUT	M5	J1, pin D1	Indicate that all FMC related powers are up	pulled up
FMC_PRSNT_M2C_L	IN	E9	J1, pin H2	Indicate if FMC installed	Low when FMC present, CPLD weak pullup enabled
FMC_SCL	OUT	J8	J1, pin C31	I ² C 2-wire serial bus	MUX in CPLD
FMC_SDA	INOUT	F9	J1, pin C30		
PG_FMC_VADJ	IN	J6	U1, pin 35	Indicate FMC VADJ power is up	
FF_RSTL	OUT	B9	J13, pin 6 and J18, pin 6	Reset configuration	Both FF are resetted simultaneously when pulled LOW
FFA_INTL	IN	E8	J13, pin 5	Indicate interrupt	LOW when fault condition, pulled up
FFA_MPRS	IN	C10	J13, pin 3	Indicate FF Module installed	LOW when Module present, pulled up
FFA_MSEL	OUT	C9	J13, pin 4	Select attached FF Module	Pull low to use I ² C
FFA_SCL	OUT	D6	J13, pin 8	I ² C 2-wire serial bus	MUX in CPLD
FFA_SDA	INOUT	E6	J13, pin 7		
FFB_INTL	IN	A10	J18, pin 5	Indicate interrupt	LOW when fault condition, pulled up
FFB_MPRS	IN	A11	J18, pin 3	Indicate FF Module installed	LOW when Module present, pulled up
FFB_MSEL	OUT	B10	J18, pin 4	Select attached FF Module	Pull low to use I ² C
FFB_SCL	OUT	D8	J18, pin 8	I ² C 2-wire serial bus	MUX in CPLD
FFB_SDA	INOUT	A9	J18, pin 7		
CPLD_IO_1	IN	B12	JB1, pin 88	(M)IOs from 4x5 Module	(M)IOs used for ETH PHY LEDs
CPLD_IO_2	IN	A12	JB1, pin 92	(M)IOs from 4x5 Module	
M10_RST		D1	TP22		Not used
M10_RX		E4	TP24		
M10_TX		E3	TP23		
EN1	OUT	D11	JB1, pin 27	Enable on module power	Depends on module, on some similar to reset.
MODE	OUT	B11	JB1, pin 31	Boot Mode selection	For Zynq modules only. (LOW SD, HIGH primary QSPI)
NOSEQ	OUT	E13	JB1, pin 8	Disable module CPLD power management	Depends on module. On some modules no extended CPLD power management available.
PGOOD	INOUT	C11	JB1, pin 29	Power good signal	This is only for monitoring, do not use as powerenable! Pulled up.
RESIN	OUT	E12	JB2, pin 17	Module Reset	Active LOW
M3.3VOUT	IN	M4	JB2, pin 9 and 11	Indicates module power is up	Used for periphery power enable. Floating when no module installed (no pull down).
SFPA_LOS	IN	M10	J12, pin 8	SFP signal loss	HIGH indicates signal loss

SFPA_M-DEF0	IN	F10	J12, pin 6	SFP modul absent	HIGH when module physically absent
SFPA_RS0	OUT	N10	J12, pin 7	SFP rate select RX	LOW for 1000BASE-SX, HIGH for 10GBASE-SR
SFPA_RS1	OUT	M11	J12, pin 9	SFP rate select TX	LOW for 1000BASE-SX, HIGH for 10GBASE-SR
SFPA_SCL	OUT	L10	J12, pin 5	I ² C 2-wire serial bus	MUX in CPLD
SFPA_SDA	INOUT	N9	J12, pin 4		
SFPA_TX_DIS	OUT	M9	J12, pin 3	SFP transmitter disable	HIGH disables transmitter
SFPA_TX_FAULT	IN	G9	J12, pin 2	Indicates SFP laser fault	HIGH indicates fault
VID0_FMC_VADJ	OUT	E10	U1, pin 34	FMC_VADJ Voltage select	Chip internal pulled up
VID1_FMC_VADJ	OUT	J7	U1, pin 33		
VID2_FMC_VADJ	OUT	L5	U1, pin 32		
VID0	IN	K6	S2-1	For FMC_VADJ Voltage select	
VID1	IN	N5	S2-2		
VID2	IN	N4	S2-3		
FMC_JTAG	IN	L3	S2-6	Select FMC JTAG port	
CM0	IN	M3	S2-7	SoM enable power	
CM1	IN	L2	S2-8	SoM Bootmode	
CM2	IN	K2	S3-1	disable SoM pwersequenzing	
USR0	IN	K1	S3-2	FMC VADJ power enable	also if no FMC installed
USB_OC	IN	D9	U12, pin 5		
EN_5VSATA	OUT	E1	U15, pin 1	Enable/Disable SATA pin 7 power	
OC_VSATA	IN	F1	U15, pin 2	Overcurrent detection SATA pin 7 power	
BUTTON	IN	N6	S1	Module reset button	
SD-CD	IN	M1	J8, pin 9	SD-Card card detect switch	Currently not used
LED1	OUT	J5	D1	user LED	
LED2	OUT	K5	D2		
LED_D4	OUT	C2	D4	Status LED	
PHY_LED1	OUT	D12	J9	Phy LEDs	
PHY_LED1R	OUT	C13	J9		
PHY_LED2	OUT	B13	J9		
PHY_LED2R	OUT	C12	J9		
A_00_N	IN	J10	JB1, pin 38	SDA IN	"three wire" I ² C
A_00_P	IN	K10	JB1, pin 36	SCL IN	"three wire" I ² C
A_01_N	OUT	L12	JB1, pin 35	TX data	RGPIO
A_01_P	OUT	K11	JB1, pin 37	SDA OUT	"three wire" I ² C
A_02_N	IN	J12	JB1, pin 41	RX CLK	RGPIO
A_02_P	IN	K12	JB1, pin 39	RX data	RGPIO
A_03_N		H10	JB1, pin 44	Module to CPLD communication	currently not used
A_03_P		J9	JB1, pin 42		
A_04_N		H13	JB1, pin 47		

A_04_P		J13	JB1, pin 45		
A_05_P	IN	H9	JB1, pin 55		
A_05_N	IN	H8	JB1, pin 57	PHY LEDs	Have to be Forwarded on SoM to this pins.
A_06_P	IN	G13	JB1, pin 51		
A_06_N	IN	G12	JB1, pin 49	I2C GPIO MUX 0	I2C MUX also used for FireFllys MSEL
A_07	IN	L13	JB1, pin 34	I2C GPIO MUX 1	

SC CPLD ports

Functional Description

Power Management

The M3_3VOUT rail of the attached SoM is used to power up the powerrails on TEF1002. further dependencies are given in the table below:

Port /Signal	depends on (RGPIO not aktive)	additional when RGPIO aktive	Description	Remark
EN_PER	M3_3VOUT	rgpio_out_data_i(15)	Enable periphery power 3V3_PER	via PWR_EN_Signal
FMC_PWR_set	M3_3VOUT	rgpio_out_data_i(16)	Signal indicate FMC enable	
EN_FMC	FMC_PWR_set and NOT(FMC_PRSENT_M2C_L)	rgpio_out_data_i(17)	Enable switched 3.3V FMC power	
FAN_FMC_EN	FMC_PWR_set and NOT(FMC_PRSENT_M2C_L)	-	Enable FMC FAN	
EN_FMC_VADJ	(FMC_PWR_set and NOT(FMC_PRSENT_M2C_L)) or (USR0 and FMC_PRSENT_M2C_L)	-	Enable IO power FMC_VADJ	USR0 dip switch S3-2 can be used to enable FMC_VADJ when no FMC installed
EN5VSATA	if((OC_VSATA = '0') or (OC_SATA_DISABLED = '1')) then EN5VSATA <= '0'; OC_SATA_DISABLED <= '1'; else EN5VSATA <= M3_3VOUT; end if;	-	Enable 5V SATA on pin 7	Implemented with latch, when disabled, will be disabled until board power cycle.
FMC_PG_C2M	FMC_PWR_set and NOT(FMC_PRSENT_M2C_L) and PG_FMC_VADJ	-	Indicate that all FMC related powers are up	

Power Management

Status LED

The Status LED D4 is utilized in the following way:

Sequenz		Description
*0000000	1 times fast blink with a break	SOM PGOOD fail
**000000	2 times fast blink with a break	not used
***00000	3 times fast blink with a break	FMC power Error
****0000	4 times fast blink with a break	SATA pin 7 overcurrent ERROR
*****000	5 times fast blink with a break	USB Power Error
*****00	6 times fast blink with a break	Firefly A or B Error

*****o	7 times fast blink with a break	SFPA_TX_FAULT or SFPA_LOS
ON	LED ON	All OK

Status LED description

FMC VADJ Power

Three of the dip switches are linked to the voltage selection signals of FMC_VADJ:

	VID0, S2-1	VID1, S2-2	VID2, S2-3
3.3V	OFF	OFF	OFF
2.5V	ON	OFF	OFF
1.8V	OFF	ON	OFF
1.5V	ON	ON	OFF
1.25V	OFF	OFF	ON
1.2V	ON	OFF	ON
0.8V	OFF	ON	ON

FMC_VADJ selection

SFP control

SFP control signals are handled by RGPIO:

OUTPUT	INPUT	Function	Notes
rgpio_in_data_i(19)	SFPA_TX_FAULT	Transmitter fault	'high' when fault detected
rgpio_in_data_i(18)	SFPA_MDEF0	Module absent	'high' when absent
rgpio_in_data_i(17)	SFPA_LOS	Signal Loss	'high' when signal loss
SFPA_TX_DIS	rgpio_out_data_i(22)	Transmitter disable	Disable transmitter when 'high'
SFPA_RS0	rgpio_out_data_i(21)	Select receive signal rate	
SFPA_RS1	rgpio_out_data_i(20)	Select transmit signal rate	

Connection SFP Control

FFA & FFB control

When RGPIO is active the FF resets are driven low via rgpio_out_data_i(23).

For FF I2C see [I2C chapter](#). Module Present and Interrupt signals are forwarded to SoM via RGPIO ports:

OUTPUT to SoM	Signal INPUT	Function	Notes
rgpio_in_data_i(23)	FFA_MPRS	Module present	active low
rgpio_in_data_i(22)	FFB_MPRS	Module present	active low
rgpio_in_data_i(21)	FFA_INTL	Interrupt output	Open collector output driven low when an Interrupt occurs.
rgpio_in_data_i(20)	FFB_INTL	Interrupt output	Open collector output driven low when an Interrupt occurs.

Connection FF Control

PCIE

The PCIeexpress signal "PERST#" is forwarded to the SoM using signal CPLD_IO_1 (corresponding to B2B pin JB1-88).

CPLD_IO_1 <= (PCIE_PERST and M3_3VOUT); -- forward PCIE PERST# to SOM

As long as RGPIO is not enabled, LED1 shows the inverted status of the PCIE_PERST signal (See [USR LED](#)).

JTAG MUX

The following table summarizes the JTAG MUX. Only FMC and SoM JTAG have to be handled in the CPLD explicitly. Discrimination between Module CPLD and Module SOC/FPGA are done via hard connected dip switch. Same is true for TEF1002 CPLD MAX10.

Signal	JTAGEN S2-4	M_JTAGEN S2-5	FMC_JTAG S2-6
CPLD MAX 10 (header J5)	ON	X	X
4x5 SoM CPLD (micro USB J10)	OFF	ON	OFF
4x5 SoC/FPGA (micro USB J10)	OFF	OFF	OFF
FMC (micro USB J10)	OFF	X	ON

JTAG selection

Module control

The module control signals are connected to dip switches:

Signal OUTPUT to SoM	Signal INPUT	Function	Notes
EN1	CM0	SoM enable power	"high" when Dip ON. See SoM TRM for further description.
NOSEQ	CM1	disable SoM powerseq	"high" when Dip ON. See SoM TRM for further description.
MODE	CM2	SoM Bootmode	"high" when Dip ON. See SoM TRM for further description.

Connection SoM Control

RESET

The push button signal is connected to the RESIN signal of the SoM (low active reset).

I²C and MUX

The SEL vector is used to select different I2C devices:

device	SEL	Notes
SFPA	00	
FMC	01	
FFA	10	also used for FFA_MSEL

FFB	11	also used for FFB_MSEL
-----	----	------------------------

Connection I2C to SoM

A "three wire" I²C interface is used to connect the CPLD I2C to the SoM:

VHDL Port name	Direction	SC CPLD Pin	Connected to	Function	Notes
A_00_N	IN	J10	JB1, pin 38	SDA IN	"three wire" I ² C
A_00_P	IN	K10	JB1, pin 36	SCL IN	"three wire" I ² C
A_01_P	OUT	K11	JB1, pin 37	SDA OUT	"three wire" I ² C

Connection I2C to SoM

The devices SDA are driven in the following way: DEVICE_XY_SDA <= '0' when SEL= "XY" and A_00_N='0' else 'Z';

The SDA to the SoM is generated by the logical AND connection of all devices: SDAs <= (SFPA_SDA AND FMC_SDA AND FFA_SDA AND FFB_SDA)

VHDL Port name	Direction	SC CPLD Pin	Connected to	Function	Notes
FMC_SCL	OUT	J8	J1, pin C31	I ² C 2-wire serial bus	MUX in CPLD
FMC_SDA	INOUT	F9	J1, pin C30		
FFA_MSEL	OUT	C9	J13, pin 4	Select attached FF Module	Pull low to use I ² C
FFA_SCL	OUT	D6	J13, pin 8	I ² C 2-wire serial bus	MUX in CPLD
FFA_SDA	INOUT	E6	J13, pin 7		
FFB_MSEL	OUT	B10	J18, pin 4	Select attached FF Module	Pull low to use I ² C
FFB_SCL	OUT	D8	J18, pin 8	I ² C 2-wire serial bus	MUX in CPLD
FFB_SDA	INOUT	A9	J18, pin 7		
A_01_P	OUT	K11	JB1, pin 37	SDA OUT	"three wire" I ² C
A_06_N	IN	G12	JB1, pin 49	I2C GPIO MUX 0	I2C MUX also used for FireFlies MSEL
A_07	IN	L13	JB1, pin 34	I2C GPIO MUX 1	

SC I2C MUX ports

PHY LEDs

The following signals are used to drive the PHY LEDs.

Signal	VHDLname	Function	Notes
A_05_N	PHY_LED1	drive LED	Connected to JB1-57
net_gnd	PHY_LED1R	select color	yellow
A_06_P	PHY_LED2	drive LED	Connected to JB1-51
net_gnd	PHY_LED2R	select color	green

Connection of PHY LEDs

RGPIO

The **RGPIO** is for communication between SoC and SC CPLD it handles the signals:

Signal	VHDLname	Function	Notes
SoC write (23)	FF_RSTL	Reset configuration	Both FF are resetted simultaneously when pulled LOW
SoC write (22)	SFPA_TX_DIS	SFP transmitter disable	HIGH disables transmitter
SoC write (21)	SFPA_RS0	SFP rate select RX	LOW for 1000BASE-SX, HIGH for 10GBASE-SR
SoC write (20)	SFPA_RS1	SFP rate select TX	LOW for 1000BASE-SX, HIGH for 10GBASE-SR
SoC write (19)	LED1	user LEDs	
SoC write (18)	LED2		
SoC write (17)	EN_FMC	Enable switched 3.3V FMC power	pulled down
SoC write (16)	FMC_PWR_set	Turn on FMC Power	used for EN_FMC_VADJ and FAN_FMC_EN
SoC write (15)	PWR_EN_Signal	Enable periphery power 3V3_PER	used for EN_PER
SOC read (23)	FFA_MPRS	Indicate FF Module installed	LOW when Module present, pulled up
SOC read (22)	FFB_MPRS	Indicate FF Module installed	LOW when Module present, pulled up
SOC read (21)	FFA_INTL	Indicate interrupt	LOW when fault condition, pulled up
SOC read (20)	FFB_INTL	Indicate interrupt	LOW when fault condition, pulled up
SOC read (19)	SFPA_TX_FAULT	Indicates SFP laser fault	HIGH indicates fault
SOC read (18)	SFPA_M-DEF0	SFP modul absent	HIGH when module physically absent
SOC read (17)	SFPA_LOS	SFP signal loss	HIGH indicates signal loss
SOC read (16)	SDCD	SD card detect	Low when card inserted
SOC read (15)	FMC_PRSNT_M2C_L	Indicate if FMC installed	Low when FMC present
SOC read (14)	PG_FMC_VADJ	Indicate FMC VADJ power is up	
SOC read (13)	OC_VSATA	Indicate SATA pin 7 overcurrent	
SOC read (12)	USB_OC	Indicate USB overcurrent	

Signals handled by **RGPIO**

VHDL Port name	Direction	SC CPLD Pin	Connected to	Function	Notes
A_01_N	OUT	L12	JB1, pin 35	TX data	
A_02_N	IN	J12	JB1, pin 41	RX CLK	
A_02_P	IN	K12	JB1, pin 39	RX data	

Connection **RGPIO** to SoM

USR LED

User LEDs are accesible via **RGPIO**:

Signal	VHDLname	Function	Notes
SoC write(19)	LED1	-	user defined
SoC write(18)	LED2	-	user defined

Connection of User LEDs

```
LED1 <= rgpio_out_data_i(19) when soc_rgpio_active='1' else Not(PCIE_PERST);  
LED2 <= rgpio_out_data_i(18) when soc_rgpio_active='1' else '0';
```

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Revision Changes

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV03	REV02		Clearified PCIe PERST#
<div>Error rendering macro 'page-info' Ambiguous method overloading for method jdk. proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</div>	<div>Error rendering macro 'page-info' Ambiguous method overloading for method jdk. proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]</div>			<div>Error rendering macro 'page-info' Ambiguous method overloading for method jdk. proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.</div>	

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12 Mar 2020	v.14	REV03	REV02	Martin Rohrmüller	initial version
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Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`