

TEF0003 TRM

[Download PDF version of this document.](#)

Table of Contents

- [Overview](#)
 - [Key Features](#)
 - [Block Diagram](#)
 - [Main Components](#)
 - [Initial Delivery State](#)
 - [Configuration Signals](#)
- [Signals, Interfaces and Pins](#)
 - [FMC Connectors](#)
 - [Coaxial Connectors](#)
 - [JTAG Interface](#)
- [On-board Peripherals](#)
 - [Quad SPI Flash Memory](#)
 - [EEPROM](#)
 - [Clock Sources](#)
 - [Programmable Clock Generator](#)
- [Power and Power-On Sequence](#)
 - [Power Supply](#)
 - [Power Consumption](#)
 - [Power Distribution Dependencies](#)
 - [Power-On Sequence](#)
 - [Power Rails](#)
 - [Bank Voltages](#)
- [Technical Specifications](#)
 - [Absolute Maximum Ratings](#)
 - [Recommended Operating Conditions](#)
 - [Physical Dimensions](#)
- [Currently Offered Variants](#)
- [Revision History](#)
 - [Hardware Revision History](#)
 - [Document Change History](#)
- [Disclaimer](#)
 - [Data Privacy](#)
 - [Document Warranty](#)
 - [Limitation of Liability](#)
 - [Copyright Notice](#)
 - [Technology Licenses](#)
 - [Environmental Protection](#)
 - [REACH, RoHS and WEEE](#)

Overview

The Trenz Electronic TEF0003 is a FPGA Mezzanine Card (FMC) integrated with an Artix 7 FPGA, 512 Mb Flash Memory.

Refer to <http://trenz.org/tef0003-info> for the current online version of this manual and other available documentation.

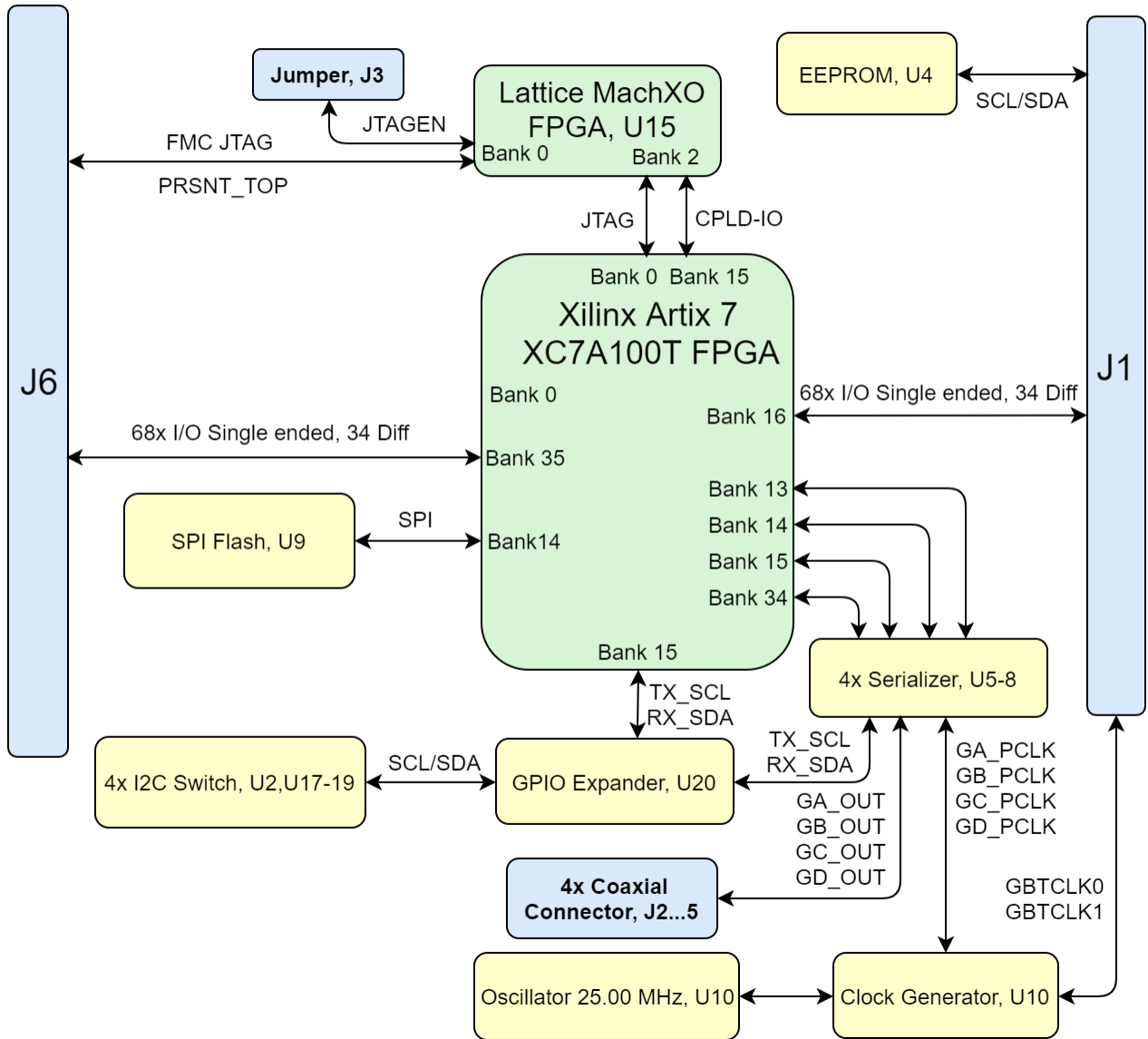
Key Features

- **FPGA:** Xilinx Artix 7 (XC7A100T)
 - Package: FGG484 (Compatible with
 - Speed: -1 (Slowest)
 - Temperature: Industrial Grade (–40°C to +100°C)
- **RAM/Storage:**
 - 1x NOR SPI FLASH (128M x 4)
 - 1x EEPROM (16K x 8)
- **On Board:**

- 4x Deserializer IC (3.12 Gbps)
 - 4x I²C and SMBus I/O Expander
 - 1x Programmable Clock Generator
 - 1x Clock Generator
- **Interface:**
 - 2x VITA 57 SEAM/SEAF Series
 - 4x Coaxial Connectors
- **Power:**
 - 4x Voltage Regulators
 - 3.3 Supply Voltage
- **Dimension:**
 - 72 mm x 65 mm

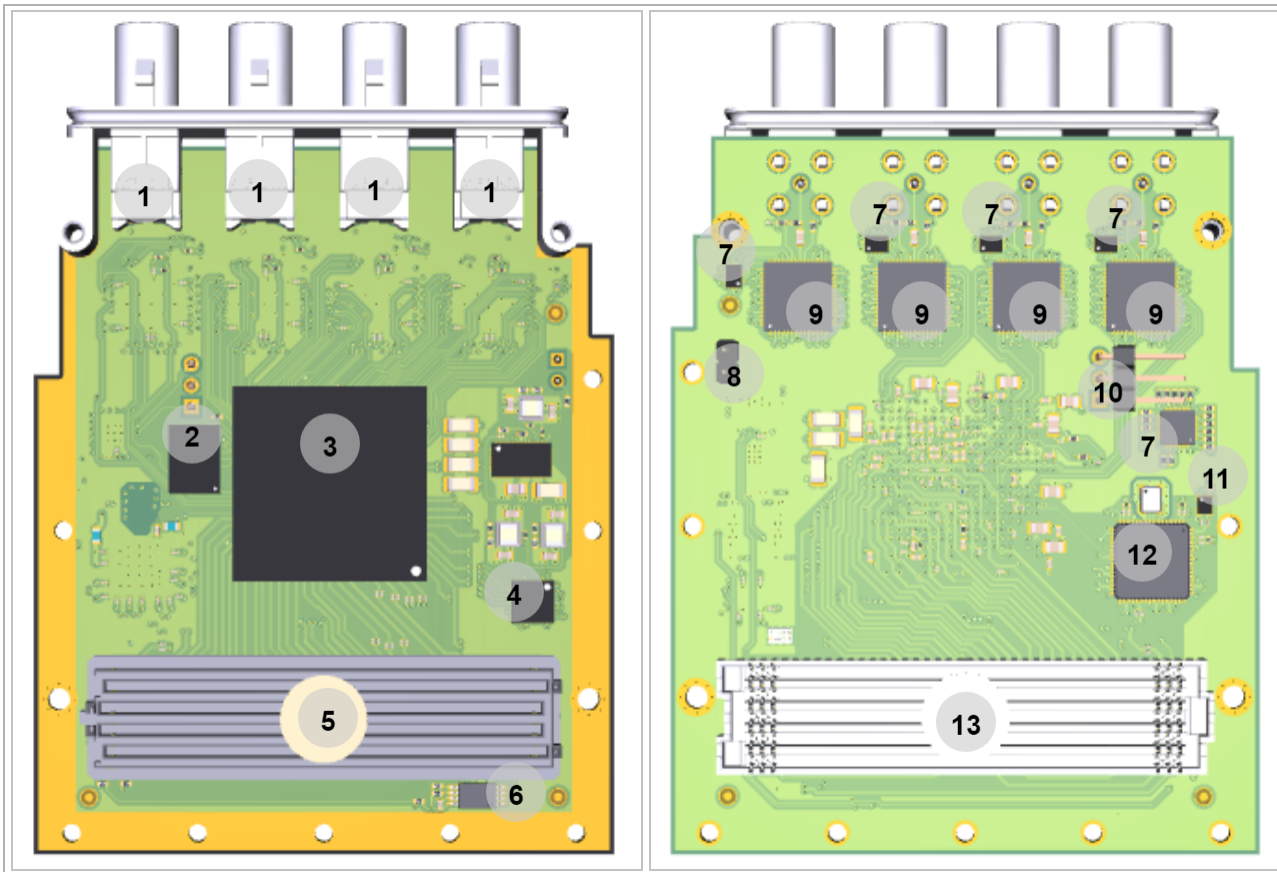
Block Diagram

TEF0003



TEF0003 block diagram

Main Components



TEF0003 main components

1. Coaxial Connectors, J2-5
2. SPI Flash, U9
3. Xilinx Artix 7 FPGA, U1
4. Lattice MachXO FPGA, U15
5. FMC Adapter, J1
6. EEPROM, U4
7. I2C Switches, U2, U17-20
8. Jumper, J7
9. Serializer, U5-8
10. Connector Header, J8
11. Oscillator 25MHz, U11
12. Programmable Clock Generator, U10
13. FMC Adapter, J6

Initial Delivery State

Storage device name	Content	Notes
SPI Flash	Not programmed	
EEPROM	Not Programmed	
Clock Generator	Programmed	

Initial delivery state of programmable devices on the module

Configuration Signals

MODE Signal State M[2:0]	Boot Mode	Note
110	Master SPI	It is Fixed

Boot process.

Signal	Description	Note
PRSNT_TOP	Lattice MachXO Configuration Pin	
PROG_B	Artix 7 Configuration Pin	Pulled up to 1.8

Reset Process.

Signals, Interfaces and Pins

FMC Connectors

FPGA bank number and number of I/O signals connected to the FMC Connectors J1 and J6 which are located on top and bottom of the board.

FPGA	FPGA Bank	Connector Designator	I/O Signal Count	Voltage Level	Notes
Artix 7, U1	16	J1B	68 Single Ended, 34 Differential	1.8V	
	35	J6B	68 Single Ended, 34 Differential	1.8V	
Lattice MachXO, U	0	J1F	4 Single Ended	3.3V	CPLD
	0	J6F	4 Single Ended	3.3V	CPLD

General PL I/O to FMC Connectors information

Coaxial Connectors

Designator	Schematic	Connected to	Notes
J2	GA_OUT	Serializer, U5	
J3	GB_OUT	Serializer, U6	
J4	GC_OUT	Serializer, U7	
J5	GD_OUT	Serializer, U8	

Coaxial Connectors information

JTAG Interface

The Lattice MachXO (U15) is available to meet the requirement of a CPLD, JTAG access to the MachXO is available through FMC Adapter J6. JTAG access to the Artix 7(U1) is available via MachXO, Bank 2.

JTAG Signal	B2B Connector	Notes
FMC_TMS	J6F-TCK	

FMC_TDI_TOP	J6F-J1-TDI	
FMC_TDO_TOP	J6F-TDO	
FMC_TCK	J6F-TCK	
JTAGEN	Pulled down	

CPLD JTAG pins connection

JTAG Signal	Connected to	Note
TMS	Lattice MachXO, U15 BankArtix 7 FPGA, U1	Bank 2 Bank 0
TDI	Lattice MachXO, U15 Artix 7 FPGA, U1	Bank 2 Bank 0
TDO	Lattice MachXO, U15 Artix 7 FPGA, U1	Bank 2 Bank 0
TCK	Lattice MachXO, U15 Artix 7 FPGA, U1	Bank 2 Bank 0
INIT	Artix 7 FPGA, U1	Pulled up to 1.8

JTAG pins connection

On-board Peripherals

Chip/Interface	Designator	Notes
SPI Flash	U9	
EEPROM	U4	
Oscillators	U11	
Programmable Clock Generator	U10	

On board peripherals

Quad SPI Flash Memory

TEF0003 is equipped with a 512Mb Serial NOR Flash (x1/x2/x4) which is provided to store an application in the SPI Flash memory in order to boot the module. The SPI Flash data is connected to Artix 7 via FPGA Bank 14.

Schematic	U9 Pin	Notes
SPI-CS	CS	
SPI-CLK	CLK	
SPI-DQ0	DI/IO0	
SPI_DQ3	HOLD/IO3	
SPI-DQ2	WP/IO2	

SPI-DQ1	DO/IO1	
1.8V	VCC	

Quad SPI interface MIOs and pins

EEPROM

A microchip serial EEPROM (U4) is provided for IPMI data. It is accessible via the LPC FMC connector J1 (SCL, SDA).

U4 Pin	FMC Pcam Adapter	Schematic	Notes
SCL	J1F-SCL	FMC_SCL	
SDA	J1F-SDA	FMC_SDA	
A0	J1F-GA0	GA0	
A1	J1F-GA1	GA1	
A2	-	-	Pulled Low
WP	-	-	Pulled Low

I2C EEPROM interface MIOs and pins

I2C Address	Designator	Notes
0xA0	U4	Write operations are enabled

I2C address for EEPROM

Clock Sources

Designator	Description	Frequency	Note
U11	Oscillator	25.00 MHz	
U10	Programmable Clock Generator	Variable	

Oscillators

Programmable Clock Generator

There is a Silicon Labs I²C programmable clock generator on-board (U10) in order to generate reference clocks for the module. Programming can be done using I²C via PIN header J8. The I²C Address is 0x69.

Si5345A Pin	Signal Name / Description	Connected To	Direction	Note
IN0	Reference input clock.	U11	Input	25.00 MHz oscillator, SiT8008BI
IN1	FMCT_GBTCLK0	J6E	Input	FMC Pcam Adapter
IN2	FMCT_GBTCLK1	J6E	Input	FMC Pcam Adapter
IN3	FMCT_CLK0	J6E	Input	FMC Pcam Adapter
XAXB	-	GND	Input	54.00 MHz CX3225SB
SCLK	PLL_SCL	J8, U20	Input	EEPROM
SDA	PLL_SDA	J8, U20	Input	EEPROM

OUT0	GA_PCLK	U5/U1	Output	FPGA bank 15
OUT1	GB_PCLK	U6/U1	Output	FPGA bank 15
OUT2	GC_PCLK	U7/U1	Output	FPGA bank 15
OUT3	GD_PCLK	U8/U1	Output	FPGA bank 15
OUT4	CLK4_P	U1H	Output	
OUT5	GBTCLK0	J1E/J6E	Output	
OUT6	GBTCLK1	J1E/J6E	Output	
OUT7	GBTCLK0	J1E	Output	
OUT8/OUT9	CLK8/CLK9	Pulled low	Output	

Programmable Clock Generator Inputs and Outputs

Power and Power-On Sequence

Power Supply

Power supply with minimum current capability of 3 A for system startup is recommended.

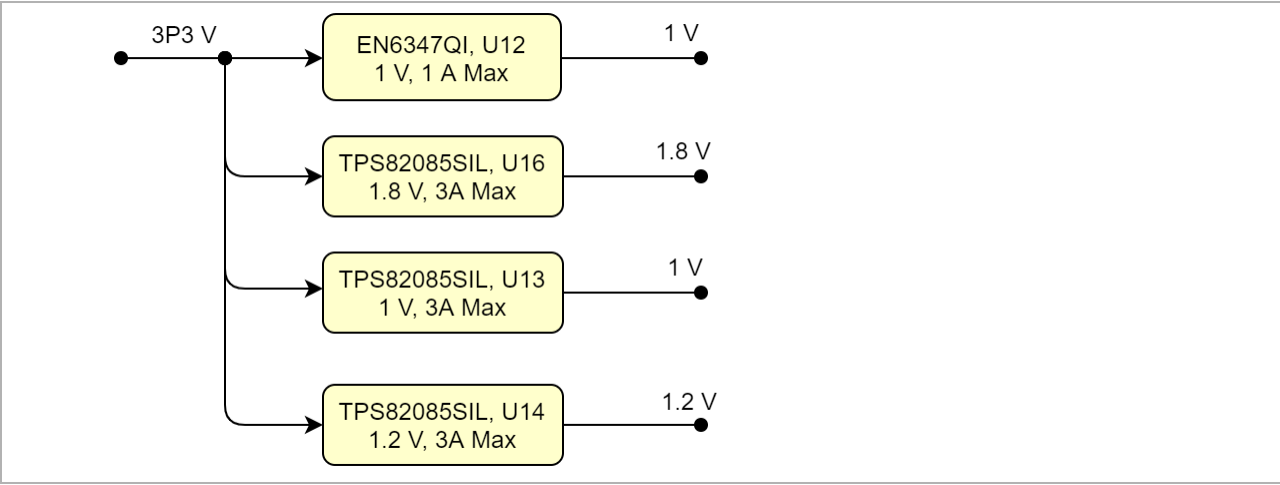
Power Consumption

Power Input Pin	Typical Current
3P3V	TBD*

Power Consumption

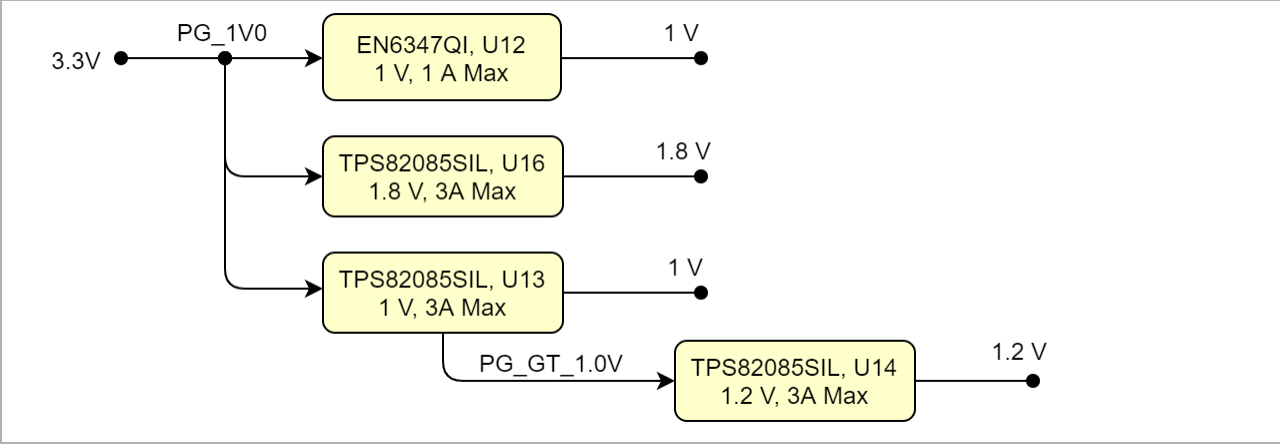
* TBD - To Be Determined

Power Distribution Dependencies



Power Distribution

Power-On Sequence



Power Sequency

Power Rails

Power Rail Name	FMC Adapter J1G Pin	FMC Adapter J6G Pin	Direction	Notes
12V	C35, C37	C35, C37	Input	
3P3VAUX	D32	D32	Input	
3P3V	D36, D38, D40, C39	D36, D38, D40, C39	Input	
VREFA	H1	H1	Input	
VREFB	K1	K1	Input	
VIOB	J39, K40	J39, K40	Input	
VADJ	H40, G39, F40, E39	H40, G39, F40, E39	Input	

Module power rails.

Bank Voltages

Bank	Schematic Name	Voltage	Notes
Bank 13	VCCO_13	1.8 V	
Bank 14	VCCO_14	1.8 V	
Bank 15	VCCO_15	1.8 V	
Bank 16	VCCO_16	VADJ	1.8 V
Bank 34	VCCO_34	1.8 V	
Bank 35	VCCO_35	VADJ	1.8 V
Bank 0	VCCO_0	1.8 V	

Zynq SoC bank voltages.

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
3P3V	Input Supply Voltage	-0.5	3.75	V
T_STG	Storage Temperature	-40	85	°C

PS absolute maximum ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

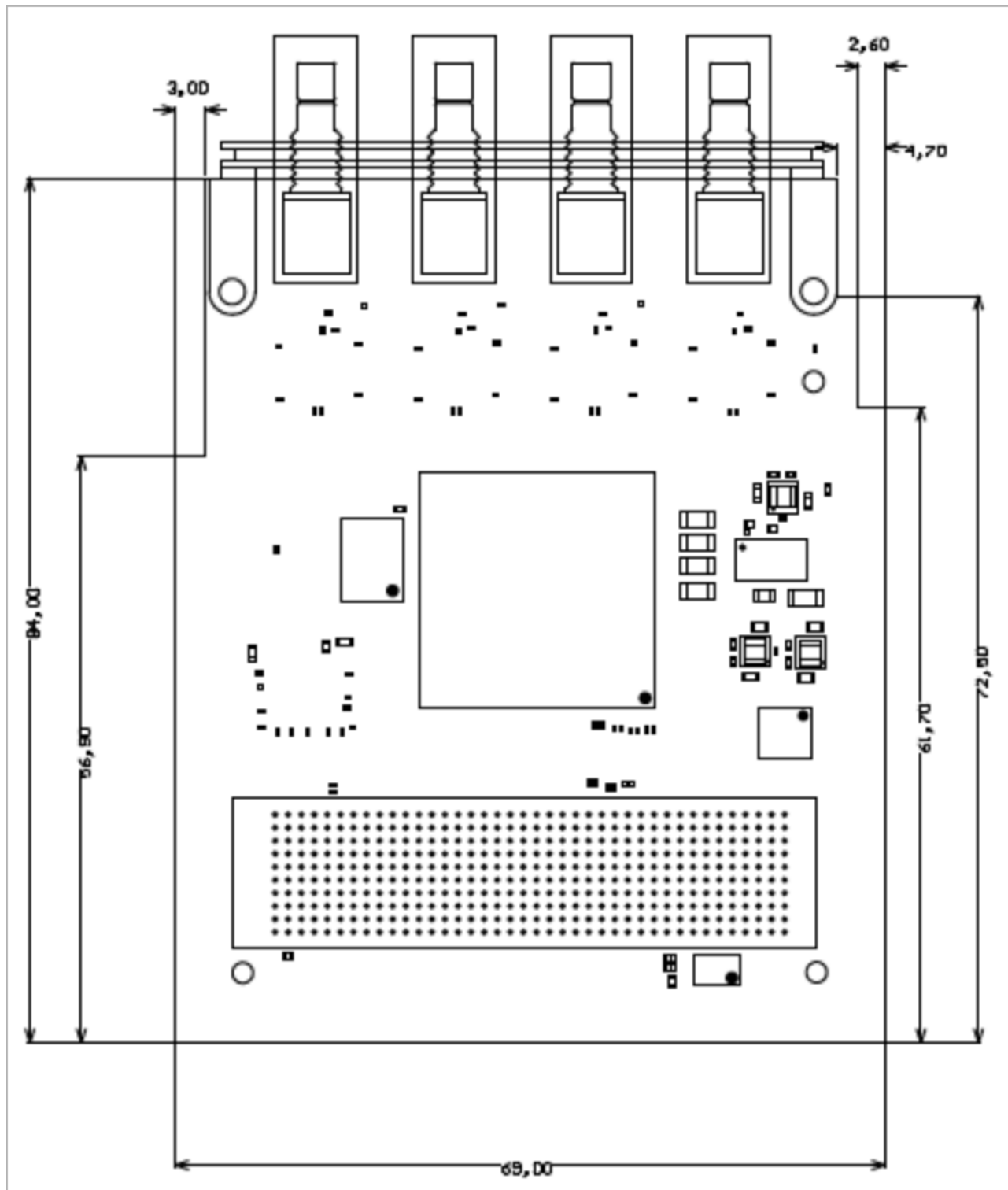
Parameter	Min	Max	Units	Reference Document
3P3V	2.375	3.465	V	
T_OPR	-40	85	°C	See MT25QU512ABB8E12-0SIT (U9) datasheet.

Recommended operating conditions.

Physical Dimensions

- Module size: 84 mm × 65 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 10 mm.

PCB thickness: 1.56 mm.



Physical Dimension

Currently Offered Variants

Trenz shop TEF0003 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Date	Revision	Changes	Documentation Link
2017-06-27	REV01	Initial Release	REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Board hardware revision number.

Document Change History

Date	Revision	Contributor	Description
------	----------	-------------	-------------

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	Initial Release
--	--	--	--

--	all	Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.\$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• --
----	-----	---	------

Document change history.

Disclaimer

Data Privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

Document Warranty

The material contained in this document is provided "as is" and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used /modified / copied only in accordance with the terms of such license.

Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`