TE0720 CPLD Firmware

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CPLD Access

Set B2B Pin JM1-89 (JTAGEN) to VDD (3.3V)

With TE0701:

- not possible on TE0701-01 up to TE0701-06

With TE0703 and TE0703 default CPLD firmware:

1. Connect MiniUSB cable to J4
2. Set DIP Switch S2-2 to OFF and S2-3 to ON position, see TE0703 CPLD - CC703S#CC703S-JTAG
3. Power ON the board
4. Run "Lattice Diamond Programmer"
5. Select "Create new project from JTAG chain" and press "OK"

With TE0705:

1. Connect MiniUSB cable to J7
2. Set DIP Switch S3-ENJTAG, S3-M1 and S3-M2 to ON position, see TE0705 CPLD#JTAG
3. Power ON the board
4. Run "Lattice Diamond Programmer"
5. Select "Create new project from JTAG chain" and press "OK"

With TE0706:

1. Connect MiniUSB cable to XMOD
2. Set DIP Switch S1-2 to OFF position, see TE0706 TRM#4-bitDIP-switch
3. Power ON the board
4. Run "Lattice Diamond Programmer"
5. Select "Create new project from JTAG chain" and press "OK"

Available CPLD Firmware

- TE0720 CPLD - Firmware description for different PCB versions and variants
  - CPLD firmware REV07 for PCB REV02 , REV03 and REV04 :
    - For all module variants as default variant located in "SC-PGM-TE0720-0304_XO2E-07_20220628" folder (Default)
      - QSPI/JTAG/SD boot modes and PUDC = 0
    - For all module variants located in "SC-PGM-TE0720-0304_XO2E-07_20220628/optional" folder (Optional)
      - QSPI/JTAG/SD boot modes and PUDC = 1
      - QSPI/SD boot modes and PUDC = 0
      - QSPI/SD boot modes and PUDC = 1
      - QSPI/JTAG boot modes and PUDC = 0

- QSPI/JTAG boot modes and PUDC = 1
- JTAG/SD boot modes and PUDC = 1
- JTAG/SD boot modes and PUDC = 1

Download

- TE0720/<PCB Revision>/Firmware/
  - Use files from the subfolders of your PCB revision

General instructions

CPLD Firmware Update - General Requirements

- Lattice Diamond or Lattice Diamond Programmer is available for free on http://www.latticesemi.com/
- Lattice compatible JTAG Programmer, for example:
  - Trenz TE0790 or Carrier with FTDI for JTAG
  - Most JTAG programmer, which used FTDI Chip to translate USB to JTAG
    - Digilent FTDI based programmer are not compatible with Lattice.
- JTAG must be connected to CPLD JTAG
- JTAG Enable Pin of CPLD must be selectable and set to VDD
- Correct CPLD Firmware (JED-File) from Trenz Electronic Download

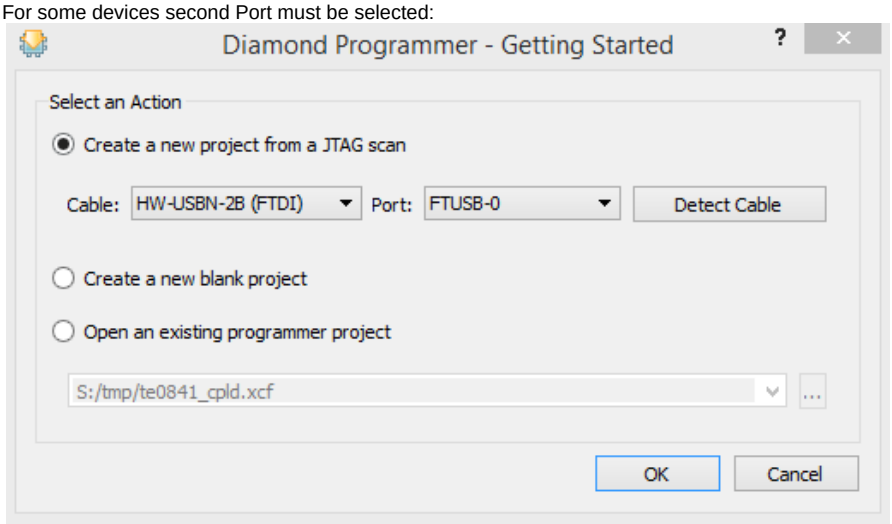
CPLD Firmware Update - General Procedure

Important:

- Connect only one JTAG device to host PC.
- Close all other JTAG programs, like Xilinx tools (on WinOS check hw_server.exe is terminated).

Procedure:

1. **Enable CPLD JTAG access** (See JTAG section on CPLD Firmware description)
2. Connect JTAG
3. Power on System
4. Open Lattice Diamond Programmer
5. Detect Cable and click "Ok"
   For some devices second Port must be selected:



6. Select Device (See CPLD Firmware overview description).
   In the most cases select the correct detected device one time (it's yellow at first on the menue)

7. Select correct Firmware from Download Area (JED File)
8. Program CPLD: 
9. **Disable CPLD JTAG access** (See JTAG section on CPLD Firmware description)
10. Restart System

More Information are available on the CPLD Firmware description and on the readme.txt included into the download zip.