TE0703 CPLD - CC703S

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Overview

CPLD Device with designator U5: LCMX02-1200HC. CC703S is minimum startup design.

Feature Summary

- JTAG
- UART
- Power
- Boot Mode
- Reset
- SD
- LED

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Pullup/Down	Bank Power	Description
ACBUS4		141			/ currently_not_used
ACBUS5		140			/ currently_not_used
ADBUS4		143			/ currently_not_used
ADBUS7		142			/ currently_not_used
BCBUS0		122			/ currently_not_used
BCBUS1		121			/ currently_not_used
BDBUS2		133			/ currently_not_used
BDBUS3		132			/ currently_not_used
BDBUS4		128			/ currently_not_used
BDBUS5		127			/ currently_not_used

BDBUS6		126			/ currently_not_used
BDBUS7		125			/ currently_not_used
CM0	in	76	UP	3.3V	DIP switch S2-2 / used as JTAG Selection/ If CM0 set to high (S2-2 OFF) Access to CPLD of module otherwise access to FPGA of module.
CM1	in	75	UP	3.3V	DIP switch S2-1 / Used to change PGOOD pin state /If Cm1 set to high (S2-1 OFF) PGOOD = '1' otherwise '0'
E_SD_CMD		110			/ currently_not_used
E_SD_DAT0		106			/ currently_not_used
E_SD_DAT1		107			/ currently_not_used
E_SD_DAT2		112			/ currently_not_used
E_SD_DAT3		111			/ currently_not_used
E_SD_SCLK		109			/ currently_not_used
EN1	out	81	NONE	3.3V	B2B Power Enable/ For TE0715 module is connected to M-TDI JTAG pin for programming the CPLD of TE0715, if optional jed file is programmed on CPLD of TE0703.
FL_0	inout	28			LED (D3-red) / Status / not connected on REV02,REV03, REV04
FL_1	inout	27			LED (D4-green) / Status / not connected on REV02,REV03, REV04
FT_B_RX	out	138	NONE	3.3V	FTDI UART
FT_B_TX / BDBUS0	in	139	UP	3.3V	FTDI UART

JTAGEN		120			Enable JTAG access to CPLD for Firmware update (zero: normal IOs, one: CPLD JTAG access). Selectable over S2-3
M_TCK	in	131	NONE	3.3V	JTAG from/to FTDI
M_TDI	in	136	NONE	3.3V	JTAG from/to FTDI
M_TDO	out	137	NONE	3.3V	JTAG from/to FTDI
M_TMS	in	130	NONE	3.3V	JTAG from/to FTDI
MIO0	in	94	UP	3.3V	DIP-S4 and B2B Pin / Used as Boot Mode
MIO10		98			/ currently_not_used
MIO11		97			/ currently_not_used
MIO12	in	100	NONE	3.3V	B2B-Module UART2 TX
MIO13	out	99	NONE	3.3V	B2B-Module UART2 RX
MIO14	out	105	NONE	3.3V	B2B-Module UART RX
MIO15	in	95	NONE	3.3V	B2B-Module UART TX
MIO9	out	96	NONE	3.3V	SD_CD / not usable as SD_CD on REV 02,REV03, REV04
MODE	out	83	NONE	3.3V	Boot Mode Pin. Switch Boot mode of Module/ For TE0715 module is connected to M-TCK JTAG pin for programming the CPLD of TE0715, if optional jed file is programmed on CPLD of TE0703.
NOSEQ	inout	78	UP	3.3V	Add Pullup only / For TE0715 module is connected to M-TMS JTAG pin for programming the CPLD of TE0715, if optional jed file is programmed on CPLD of TE0703.

PGOOD	inout	82	UP	3.3V	Add Pullup used for Status / Boot Mode Pin. Switch Boot mode of Module /For TE0715 module is connected to M-TDO JTAG pin for programming the CPLD of TE0715, if optional jed file is programmed on CPLD of TE0703.
PHY_LED1	out	86	DOWN	3.3V	Status / currently _not_used
PHY_LED1R	out	92	NONE	3.3V	Status / currently _not_used
PHY_LED2	out	85	NONE	3.3V	Status / currentl y_not_used
PHY_LED2R	out	91	NONE	3.3V	Status / currently _not_used
PROGMODE	out	104	UP	3.3V	Enable B2B Module JTAG access to CPLD for Firmware update
RESIN	out	119	NONE	3.3V	Module Reset Pin on B2B connector
S1	in	114	UP	3.3V	Push Button / Used as module Reset
SD_CD	in	93	UP	3.3V	Forward to MIO 9 / not connected on REV02,REV03, REV04
SD_SEL	out	113	NONE	3.3V	Set to GND / cur rently_not_used
TCK_B	out	1	NONE	3.3V	JTAG from/to Module
TDI_B	out	3	NONE	3.3V	JTAG from/to Module
TDO_B / C_TDO	in	2	UP	3.3V	JTAG from/to Module
TMS_B	out	4	NONE	3.3V	JTAG from/to Module
ULED1 / LED1	out	117	NONE	3.3V	LED (D1-red) / UART Monitoring
ULED2 / LED2	out	115	NONE	3.3V	LED (D2-green) / UART Monitoring
USB_OC		73			/ currently_not_u sed
X0		39			/ currently_not_u sed

X1		38			/ currently_not_used
X10		49			/ currently_not_used
X11		50			/ currently_not_used
X12		52			/ currently_not_used
X13		54			/ currently_not_used
X14		55			/ currently_not_used
X15		56			/ currently_not_used
X16	in	59	UP	3.3V	UART2 on VG connector J2
X17	out	60	NONE	3.3V	UART2 on VG connector J2
X2		40			/ currently_not_used
X3		41			/ currently_not_used
X4		42			/ currently_not_used
X5		43			/ currently_not_used
X6		44			/ currently_not_used
X7		45			/ currently_not_used
X8		47			/ currently_not_used
X9		48			/ currently_not_used

Functional Description

JTAG

JTAG signals routed directly through the CPLD to module in B2B connector. Access between CPLD and module can be multiplexed via JTAGEN (logical one for CPLD, logical zero for module). TE0703 CPLD can be selected with JTAGEN (DIP-S2-3). Module FPGA/CPLD access can be switched with PROGMODE which is driven by CM0 (DIP-S2-2).CM0 is pulled up with CPLD.

If used SoM on the carrier board is TE0715, CPLD of TE0703 must be programmed a different jed file to arrange CPLD JTAG pins correctly. This module is an exception. For this purpose it is defined a generic parameter in VHDL code to switch JTAG pins differently as other SoM modules. There are two jed files. CPLD of TE0715 module with default jed file for CPLD of carrier board TE0703 can not be programmed. But optional jed file exists for this purpose. In both cases default or optional jed file the following table is valid:

S2-2	S2-3	PROGMODE (S2-2)	JTAGEN (S2-3)	Description

OFF	OFF	1	1	Access to TE0703 CPLD
OFF	ON	1	0	Access to CPLD of B2B Module
ON	OFF	0	1	Access to TE0703 CPLD
ON	ON	0	0	Access to FPGA of B2B Module

Note: LED1,2,3,4 are on and PHY LEDs blink slow, if S2-2 is set to OFF.

Power

EN1 is set to one.

NOSEQ and PGOOD pulled up to VDD. NOSEQ pin is either high impedance or is used as JTAG pin to program CPLD of TE0715 module. PGOOD pin can be set or reset by user. If CM0 or CM1 set to high (S2-2 or S2-1 OFF) , PGOOD will be set to high otherwise PGOOD is set to low.

Reset

RESIN is driven by S1 (Push Button). Button is debounced.

Boot Mode

MODE pin is sourced by MIO0. MIO0 connected DIP S2-4 and B2B connector. MIO is pulled up with CPLD and can be set to GND via DIP. PGOOD pin will be used as second select pin for boot mode selection. In this case the following table can be considered:

S2-1	S2-4	PGOOD	MIO0	Description
ON	ON	0	0	JTAG boot mode
OFF	ON	1	0	SD Card boot mode, PHY LEDs glow orange
OFF	OFF	1	1	QSPI boot mode, PHY LEDs glow green

UART

Primary UART:

MIO14 is driven by BDBUS0 (FTDI RX).

BDBUS1 (FTDI TX) is driven by MIO15 .

Secondary UART:

MIO13 is driven by X16.

X17 is driven by MIO12.

SD

SD selection is set to GND (SD Card slot).

MIO9 is switched to SD_CD and its status depends on SD_CD .

LED

LED Priority is order of the description

LED	Prio 0: Power	Prio 1: Modul CPLD access*	Prio 2
LED1 (D1-red)	Blink, if Power Good is low	ON	FTDI UART RX
LED2 (D2-green)	Blink, if Power Good is low	ON	FTDI UART TX
LED3 (D3-red)	OFF	ON	User defined with B2B Pin JB2-99
LED4 (D4-green)	OFF	ON	User defined with B2B Pin JB2-90
PHY LEDs (green/orange)	Blink orange, if Power Good is low	Blink Green and orange	Green: Boot Mode set to QSPI, Orange: Boot Mode set to SD

*Attention: LED1,2,3,4 are on, if S2-2 is set to OFF. If S2-3 is OFF, TE0703 is in chain!

Appx. A: Change History and Legal Notices

Revision Changes

- REV02 to REV03
  - Oscillator frequency is changed from 12.09 MHz to 24.18 MHZ.
  - Access to CPLD of TE0715 with a generic parameter added. (For optional jed file to access CPLD of TE0715 module)
  - PGOOD used as second boot mode selector pin and connected to dip switch S2-1. PGOOD and MODE are boot mode selector pins.
  - S2-1 dip switch (CM1) functionality is changed.In HW PCB REV0 to REV04 is used for SD card detection but in HW PCB REV05 and REV06 is used to set or reset PGOOD.
  - MIO14 is connected to FTDI_RXD directly without depending on PGOOD.
  - CM1 (Dip switch S2-2) has no effect on MIO9 anymore. That means MIO9 is connected to SD_CD only and not to SD_CD and CM1.
- REV02 to older REV01
  - Enable CPLD access to module CPLD over DIP
  - Add MIO0, SD_SEL, SD_CD, NOSEQ, PGOOD, 2LEDs, PHY LEDs
  - Debounce button
  - More status LED functionality

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description

Error re Ambigu	**Error rendering macro 'page-info'** Ambiguous method overloading for method java.lang.String#replaceAll in template at line 24	REV03	REV05, REV06	**Error rendering macro 'page-info'** Ambiguous method overloading for method java.lang.String#replaceAll in template at line 24	• REV03 release • Firmware release (SC-PCM-TE0703-0506_CARRIER-03_20220815.zip) • PGOOD as secondboot mode select pin • TE0715 CPLD programming is possible
2019-11-08	v.13	REV02	REV02*,REV03*, REV04*,REV05, REV06 *some IOs are not connected *SD_CD not available, set S2-1 to on	John Hartfiel	• Typo • Note PCB REV06 support
2017-10-13	v.11	REV02	REV02*,REV03*, REV04*,REV05 *some IOs are not connected *SD_CD not available, set S2-1 to on	John Hartfiel	• REV 02 finished
2016-04-11	v.1	REV02	REV02*,REV03*, REV04*,REV05 *some unused IOs are not connected *SD_CD not available, set S2-1 to on	John Hartfiel	• Initial release
	All			John Hartfiel	

Appx. B: Legal Notices

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy244.$Proxy3572#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]