TE0703 TRM

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Overview

The Trenz Electronic TE0703 Carrier Board is a base-board for 4 x 5 SoMs, which exposes the MIO- and the PS/PL-pins of the SoM to accessible connectors and provides a whole range of on-board-components to test and evaluate Trenz Electronic 4 x 5 SoMs.

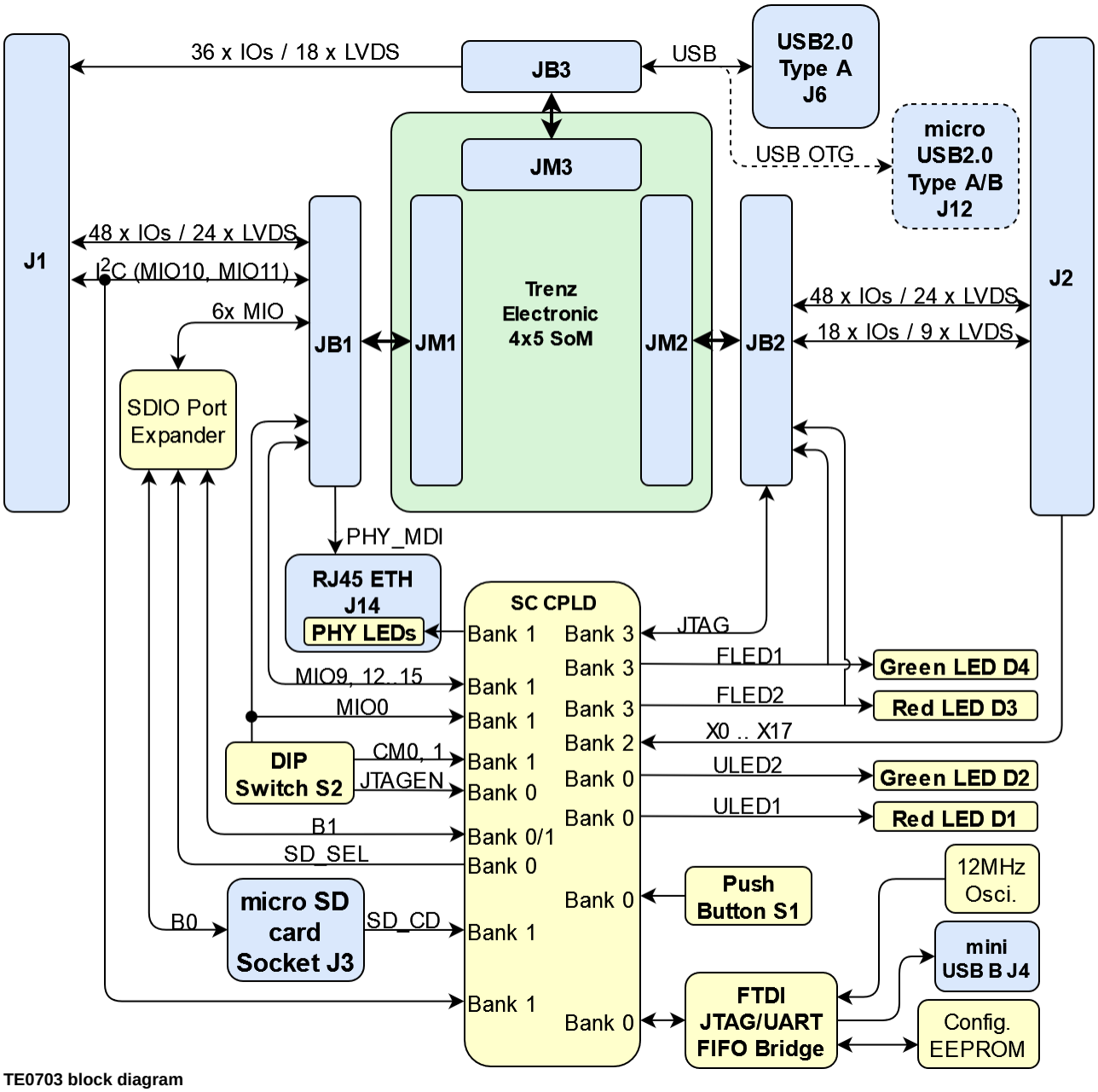
See page "4 x 5 cm carriers" to get information about the SoM's supported by the TE0703 Carrier Board.

Refer to http://trenz.org/te0703-info for the current online version of this manual and other available documentation.

Key Features

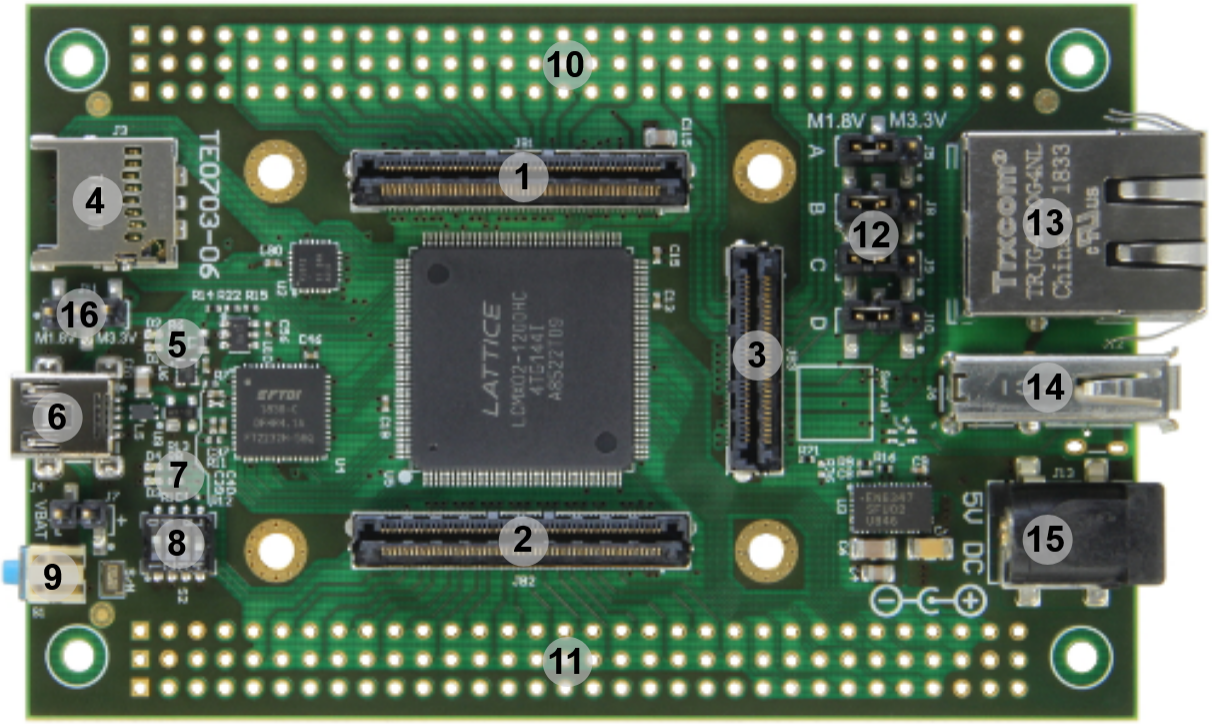
- On Board:
  - USB JTAG and UART interface (FTDI FT2232H), compatible with Xilinx tools (also with many other tools)
  - SDIO port expander with voltage-level translation
  - 4 x User LEDs
    - D1 and D2 are connected to the carrier controller, their function depends on the firmware
    - D3 and D4 are connected to the 4 x 5 module B2B connector pins, and are directly controlled by the module
  - 1 x User push button
    - Connected to "intelligent Carrier Controller (iCC)" and can be used as module reset button. Other usage possible, actual function depend on the code loaded into iCC.
  - 6 A DC-DC step-down converter with integrated inductor for 3.3V power supply
  - 4 User DIP switches
    - Enable/disable update of the "intelligent Carrier Controller"
    - MIO0 (readable signal by iCC and module)
    - 2 "mode" bits
- Interface:
  - Trenz 4 x 5 module socket (3 x Samtec LSHM series connectors)
  - Micro SD card connector - Zynq SDIO0 bootable SD port
  - 2 x VG96 backplane connectors (mounting holes and solder pads)
  - Mini USB connector (USB JTAG and UART interface)
  - RJ45 GbE connector
  - USB host connector
- Power:
  - Barrel jack for 5V power supply input
- Dimension:
  - 100 mm x 64.5 mm

Block Diagram



TE0703 block diagram

Main Components



TExxxx main components

1. Samtec Razor Beam™ LSHM-150 B2B connector, JB1
2. Samtec Razor Beam™ LSHM-150 B2B connector, JB2
3. Samtec Razor Beam™ LSHM-130 B2B connector, JB3
4. Micro SD card socket with detect switch, J3
5. LED indicators D1 and D2
6. Mini-USB type B connector, J4
7. LED indicators D3 and D4
8. Configuration DIP switches, S2 (see table under "DIP switches" section)
9. User push button (Reset), S1
10. External connector (VG96) placeholder, J1
11. External connector (VG96) placeholder, J2
12. VCCIO voltage selection jumper block, J5, J8, J9 and J10 (see "Power and Power-On Sequence" section)
13. Trxcom 1000Base-T Gigabit RJ45 Magjack, J14 with 4 integrated LEDs
14. USB type A receptacle, J6 (optional micro USB 2.0 type A/B receptacle available, J12)
15. 5V power connector jack, J13
16. SD IO voltage (VCCA) selection jumper J11

Initial Delivery State

Storage device name	Content	Notes
FTDI chip configuration EEPROM U10	Xilinx License	Do not overwrite, see warning in related section
System Controller CPLD U5	SC CPLD Firmware	-

Initial delivery state of programmable devices on the module

Board is shipped in following configuration:

- VCCIO voltage selection jumpers are all set to 1.8 V.

- SD IO Voltage jumper J11 is set to 1.8V.
- S1 switch configured as reset button in CPLD.
- Two VG96 backplane connectors are not soldered to the board, but they are included in the package as separate components.
- S2 DIP switches are configured as follows:

Switch	Position	Description
S2-1	ON	Mode control MC1.
S2-2	ON	FPGA access on module (need also S2-3 ON)
S2-3	ON	FPGA access on module (need also S2-2 ON)
S2-4	OFF	Boot mode set to QSPI.

Initial delivery state DIP switches

Different delivery configurations are available upon request.

Configuration Signals

The configuration signals are managed by the CPLD and therefore Firmware dependet. Standart configuration is given below.

Control signal	Switch /Button/ LED /Pin	Signal Schematic Names	Connecte to	Functionality	Notes
Module JTAG select	Dip switche S2-2	CM0	SC CPLD pin 75	ON: Module JTAG access (if S2-3 ON) OFF: Module CPLD JTAG access (if S2-3 ON)	TE0703 CPLD - CC703S#CC703S-JTAG
Module JTAG select	SC CPLD pin 104	PROGMODE	B2B JB1 pin 90	Module JTAG select: Module CPLD high or SoC/FPGA JTAG low ; via CPLD firmware linked to CM0	TE0703 CPLD - CC703S#CC703S-JTAG
Carrier CPLD JTAG enable	Dip switch S2-3	JTAGEN	SC CPLD pin 120	ON: SoM JTAG access OFF: Carrier SC CPLD JTAG access	TE0703 CPLD - CC703S#CC703S-JTAG
Select boot mode	Dip switche S2-4	MIO0	SC CPLD pin 94 and B2B JB1 pin 88	ON: Boot from SD Card OFF: Boot from QSPI flash on module	TE0703 CPLD - CC703S#CC703S-BootMode Boot Mode is also module dependent
Select boot mode	SC CPLD pin 83	MODE	B2B JB1 pin 31	SD-CARD (Zynq) or QSPI-Flash; via CPLD firmware linked to MIO0	TE0703 CPLD - CC703S#CC703S-BootMode Boot Mode is also module dependent
Reset	S1	S1	SC CPLD pin114	global reset	TE0703 CPLD - CC703S#CC703S-Reset
Reset	SC CPLD pin 119	RESIN	B2B JB2 pin 17	via CPLD firmware linked to S1	TE0703 CPLD - CC703S#CC703S-Reset
Moduel enable	SC CPLD pin 81	EN1	B2B JB1 pin 27	Module power enable	pulled up by CPLD
Disable CPLD power Management	SC CPLD pin 78	NOSEQ	B2B JB1 pin 8	Disable CPLD power management	pulled up by CPLD
Disable Card detect pin	Dip switche S2-1	CM1	SC CPLD pin 76	ON: Force CD Pin to module to GND OFF: Set CD Pin to module to SD CD Pin	TE0703 CPLD - CC703S#CC703S-SD
SD Card detect	SD Card Socket J3 pin 9	SD_CD	SC CPLD pin93	Low if Card detected	TE0703 CPLD - CC703S#CC703S-SD

SD Selector	SC CPLD pin 113	SD_SEL	U2 pin 24	FIXed to GND: Select SD Card (CPLD SD port not used)	TE0703 CPLD - CC703S not used

Boot process.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the B2B connector:

B2B Connector	Interfaces	I/O Signal Count	Notes
JB1	User IO	48 single ended or 24 differential	Available on J1
	I²C	2	MIO10, MIO11, available on J1
	SD IO	6	-
	primary UART	2	MIO14, MIO15; CPLD Firmware dependent
	secondary UART	2	MIO12, MIO13; CPLD Firmware dependent
	GbE PHY_MDIO	8	-
	Control Signals	7	including MIO0 and MIO9; CPLD Firmware dependent
	VBAT	1	-
JB2	User IO	36 single ended or 18 differential	Available on J1
	USB OTG	5	Including USB-VBUS and VBUS_V_EN
JB3	User IO	66 single ended or 33 differential	Available on J2
	LEDs	2	-
	JTAG	4	-
	Control Signal	1	Reset

General overview of PL I/O signals and SoM's interfaces connected to the B2B connectors

Micro SD Card Socket

Micro SD card socket is connected to the B2B connector through a Texas Instruments TXS02612 SDIO port expander for voltage translation. The Micro SD card has 3.3V signal voltage level while most 4 x 5 modules use 1.8V for the SD card interface.

Connected To	Signal Name	Notes
U5-93	SD-CD	Managed CPLD Firmware
JB1-28	SD-DAT0	-
JB1-26	SD-CMD	-
JB1-24	SD-CCLK	-
JB1-22	SD-DAT1	-
JB1-20	SD-DAT2	-
JB1-18	SD-DAT3	-

SD Card interface signals and connections

USB Interface

TE0703 board has two physical USB sockets:

- J4 as mini-USB type B socket wired to the on-board FTDI FT2232H chip.
- J6 as USB type A wired to B2B connector JB3 (USB transceiver used depends on the SoM model used). Instead of J6, a micro USB connector J12 can be assembled

USB Connector	Signal	Connected to
J4	DL_N	U4-7
	DL_P	U4-8
J6 or J12	OTG-D_P	JB3-48
	OTG-D_N	JB3-50
(J12 only)	OTG-ID	JB3-52

USB Signals

Ethernet

On-board Ethernet jack J14 pins are routed to B2B connector JB1. Ethernet jack J14 LED signals PHY_LED1, PHY_LED2, PHYLED1R and PHYLED2R are all routed to System Controller CPLD bank 1.

Ethernet PHY connection

MagJack	Signal	B2B
J14A-2	PHY_MDI0_P	JB1-3
J14A-3	PHY_MDI0_N	JB1-5
J14A-4	PHY_MDI1_P	JB1-9
J14A-5	PHY_MDI1_N	JB1-11
J14A-6	PHY_MDI2_P	JB1-15
J14A-7	PHY_MDI2_N	JB1-17
J14A-8	PHY_MDI3_P	JB1-21
J14A-9	PHY_MDI3_N	JB1-23
J14B	PHY_LED1	U5-86
J14B	PHY_LED1R	U5-92
J14C	PHY_LED2	U5-85
J14C	PHY_LED2R	U5-91

Ethernet Signals

External VG96 Connector I/Os

I/O signals connected to the B2B connector:

B2B Connector	Interfaces	I/O Signal Count	Notes
J1	User IO	48 single ended or 24 differential	From JB1 (group1)
	User IO	36 single ended or 18 differential	From JB3 (group2)
	I²C	2	
J2	User IO	48 single ended or 24 differential	From JB2 (group4)
	User IO	18 single ended or 9 differential	From JB2 (group3)
	CPLD User IO	18 single ended	Including UART 2 on X16, X17; CPLD Firmware dependent

General overview of PL I/O signals and SoM's interfaces connected to the B2B connectors

On-board Peripherals

USB to JTAG and UART bridge

TE0703 has on-board USB JTAG and UART solution based on UART/FIFO controller from FTDI (U4). FTDI EEPROM is pre-programmed with license code to support Xilinx programming tools.

Do not access the FT2232H EEPROM using FTDI programming tools, doing so will erase normally invisible user EEPROM content and invalidate stored Xilinx JTAG license. Without this license the on-board JTAG will not be accessible any more with any Xilinx tools. Software tools from FTDI website do not warn or ask for confirmation before erasing user EEPROM content.

JTAG and UART signals along with some more FTDI IOs are routed to the CPLD. See CPLD Firmware TE0703 CPLD - CC703S#CC703S for further description.

Signal	B2B Connector Pin	Note
M_TCK	U5-131	CPLD Firmware dependent TE0703 CPLD - CC703S#CC703S, dependent on Dip switches linked to Module JTAG Port on JB2.
M_TDI	U5-136	
M_TDO	U5-137	
M_TMS	U5-130	
FT_B_TX	U5-139	CPLD Firmware dependent TE0703 CPLD - CC703S#CC703S, linked to Module primary UART on JB1.
FT_B_RX	U5-138	
ADBUS7	U5-142	CPLD Firmware dependent TE0703 CPLD - CC703S#CC703S, currently not used.
ADBUS4	U5-143	
ACBUS4	U5-141	
ACBUS5	U5-140	
BDBUS2	U5-133	
BDBUS3	U5-132	
BDBUS4	U5-128	

BDBUS5	U5-127
BDBUS6	U5-126
BDBUS7	U5-125
BCBUS0	U5-122
BCBUS1	U5-121

JTAG pins connection

CPLD

TE0703-06 has a Lattice LCMXO2-1200HC as a system controller. for further function description see Firmware TE0703 CPLD - CC703S#CC703S,

SD IO Levelshifter

SD IO levelshifter (U2) is used in congntion with jumper J11 to select the correct SD IO interface voltage of the SoM.

I^{2}C Repeater

For power sequence reasons the I^{2}C bus is routed via a repater (U7) to to ensure no IOs of the SoM are driven before M3.3VOUT is up.

LEDs

There are four on-board LEDs. D3 and D4 are connected to the B2B connector JB2 pins FLED1 and FLED2 respectively and can be read by CPLD firmware. See TE0703 CPLD - CC703S#CC703S-LED.

LED	Color	Signal	Connected to	Description
D1	Red	ULED1	U5-117	FTDI UART receive activity.
D2	Green	ULED2	U5-115	FTDI UART transmit activity.
D3	Red	FLED1	JB2-99	Module LED, CPLD can read status via signal FL_0 connected via 10K.
D4	Green	FLED2	JB2-90	Module LED, CPLD can read status via signal FL_1 connected via 10K.

On-board LEDs

DIP switches

DIP switch settings are CPLD Firmware dependent, default firmware:

Switch	ON	OFF	Notes
S2-1	Set PGOOD pin to low ('0') / Force CD pin to module to high impedance ('Z')	Set PGOOD pin to high ('1') / Set CD pin to module to SD_CD pin	TE0703 CPLD - CC703S#CC703S-BootMode / TE0703 CPLD - CC703S#CC703S-SD
S2-2	Module FPGA JTAG access (if S2-3 ON)	Module CPLD JTAG access (if S2-3 ON)	TE0703 CPLD - CC703S#CC703S-JTAG
S2-3	Module FPGA/CPLD JTAG access (depends on S2-2)	Carrier CPLD JTAG access	TE0703 CPLD - CC703S#CC703S-JTAG
S2-4	Boot from SD Card (Set pin to GND)	Boot from QSPI flash on module (Set pin to VDD)	TE0703 CPLD - CC703S#CC703S-BootMode Boot Mode also depends on module.

Dip-Switches

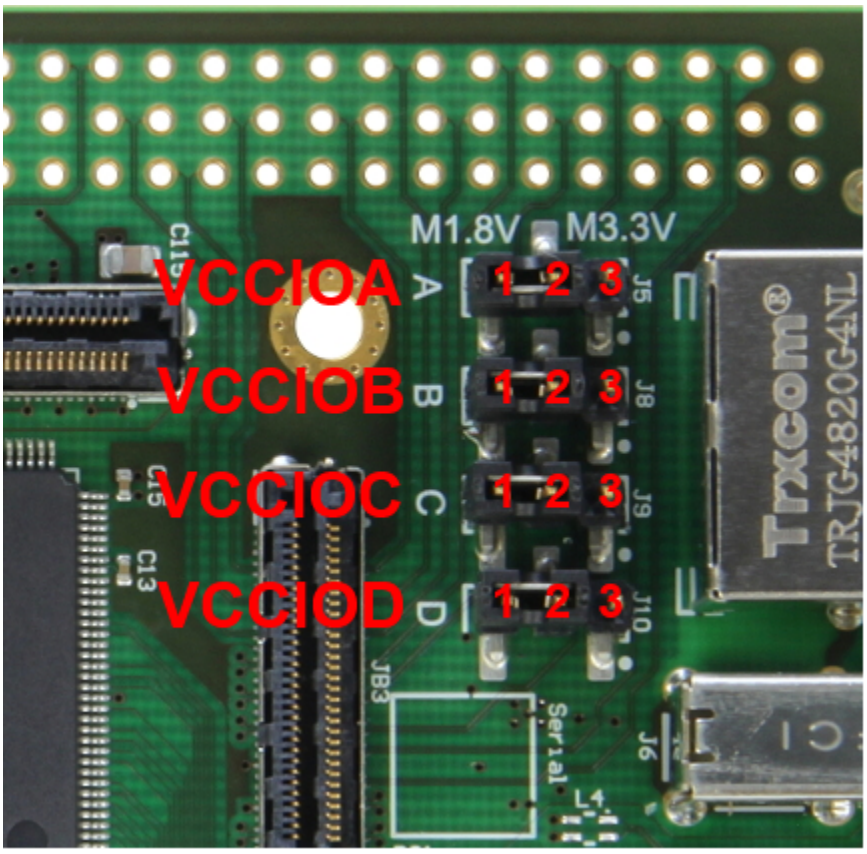
Mode status is displayed on TE0703 LEDs, see TE0703 CPLD - CC703S#CC703S-LED.

Jumper

TE0703-06 has 5 Voltage selection jumpers. Select 1.8V or 3.3V in accordenc of the attached module capabilities and your needs. Refer to the 4 x 5 Module Integration Guide for VCCIO voltages options.

Power Rail	Jumper	1.8V	3.3V	Notes
VCCIOA	J5	1-2	2-3	-
VCCIOB	J8	1-2	2-3	-
VCCIOC	J9	1-2	2-3	-
VCCIOD	J10	1-2	2-3	-
VCCA	J11	1-2	2-3	SD IO level shifter voltage selection (module side), compare with TRM of attached Module

Jumpers



TE0703 Jumper Settings

> ⚠ Take care of the VCCO voltage ranges of the particular PL IO-banks (HR, HP) of the mounted SoM, otherwise damages may occur to the FPGA. Therefore, refer to the TRM of the mounted SoM to get the specific information of the voltage ranges.
>
> It is recommended to set and measure the PL IO-bank supply-voltages before mounting of TE 4 x 5 module to avoid failures and damages to the functionality of the mounted SoM.

Power

Power supply with minimum current capability of 3A for system startup is recommended.

Power Supply

Single power supply with minimum current capability of 3A at 5V for system startup is recommended.

Power Consumption

Power Input Pin	Max Current
VIN (power connector jack J13)	4A

Power Consumption

Typical power consumption for TE0703-05 + TE0715-01 module with SD micro card inserted, Ethernet connected and link up, system booted into Linux prompt and idling is 5V / 0.55A.

Power-On Sequence

It is not allowed to feed any voltage to any external I/O pin before there is no power indication on M3.3VOUT pins. Presence of 3.3V on B2B JB2 connector pins 9 and 11 indicates that module is properly powered up and ready.

If any of the VCCIOA, VCCIOB, VCCIOC or VCCIOD will be powered through external connectors J1 or J2, then corresponding VCCIO jumper should also be removed.

Power Rails

Power Rail Name	Connector-Pin	Direction	Notes
5VIN	J13-1	in	5 V power input
VIN	-	-	5 V power input after protection
3.3V	JB1-2, 4, 6, 14, 16	out	Generatet from VIN by DCDC U3, constant 3.3V rail
M1.8VOUT	JB1-40	in	1.8V from Module.
M3.3VOUT	JB2-9, 11	in	3.3V from Module.
VCCIOA	JB1-10, 12	out	Use jumper J5 to source by M1.8VOUT or M3.3VOUT.
VCCIOB	JB2-2 ,4	out	Use jumper J8 to source by M1.8VOUT or M3.3VOUT.
VCCIOC	JB2-6	out	Use jumper J9 to source by M1.8VOUT or M3.3VOUT.
VCCIOD	JB2-8, 10	out	Use jumper J10 to source by M1.8VOUT or M3.3VOUT.
VCCA	-	-	SD IO leveshifter voltge on Module side. Use jumper J11 to source by M1.8VOUT or M3.3VOUT.
VCCJTAG	JB2-92	in	JTAG reference voltage
USB-VBUS_R	J6-1 (J12-1)	out	5V USB, derived from VIN by power switch U1

Module power rails.

Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm

	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

Connectors.

The module can be manufactured using other connectors upon request.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report_lshm-lshm-05mm_web.pdf High speed test report	07 04, 2016 by Thorsten Trenz
PDF File lshm_dv.pdf LSHM catalog page	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-X-DV-A-X-X-TR-FOOTPRINT(1).pdf Recommended layout and stencil drawing	07 04, 2016 by Thorsten Trenz
PDF File LSHM-1XX-XX.X-XX-DV-A-X-X-TR-MKT.pdf Technical drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189016-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-01.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File REF-189017-02.pdf Technical Drawing	07 04, 2016 by Thorsten Trenz
PDF File TC0923--2523_report_Rev_2_qua.pdf Design qualification test report	07 04, 2016 by Thorsten Trenz

PDF File tc0929--2611_qua(1).pdf Shock and vibration report 07 04, 2016 by Thorsten Trenz

Download All

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference document
5VIN supply voltage	-0.3	7	V	MP5010A, EN6347QI data sheet
Storage temperature	-40	+100	°C	ROHM Semiconductor SML-P11 Series datasheet

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference document
5VIN supply voltage	4.75	5.25	V	USB2.0 specification concerning 'VBUS' voltage
Operating temperature	-40	+85	°C	FTDI FT2232H datasheet

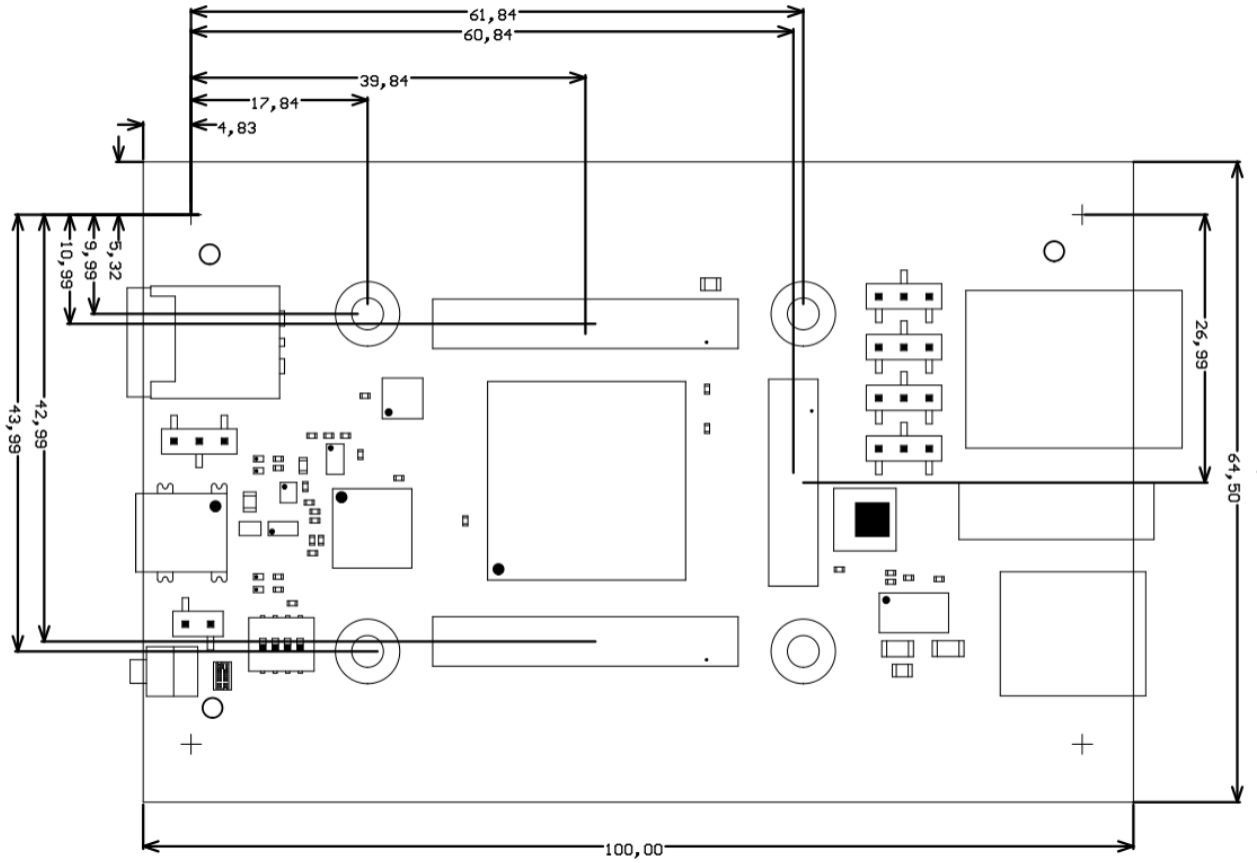
⚠ Assembly variants for higher storage temperature range are available on request.

⚠ Please check components datasheets for complete list of absolute maximum and recommended operating ratings.

Physical Dimensions

- Board size: 100 mm × 64.5 mm. Notice that the mini-USB jack on the left and ethernet RJ-45 jack on the right are hanging slightly over the edge of the PCB making the total width of the longer side approximately 106 mm. Please download the assembly diagram for exact numbers.
- Mating height of the module with standard connectors: 8 mm
- PCB thickness: 1.65 mm
- Highest parts on the PCB are USB type A jack and ethernet RJ-45 jack, approximately 15 mm. Please download the step model for exact numbers.

All dimensions are given in millimeters.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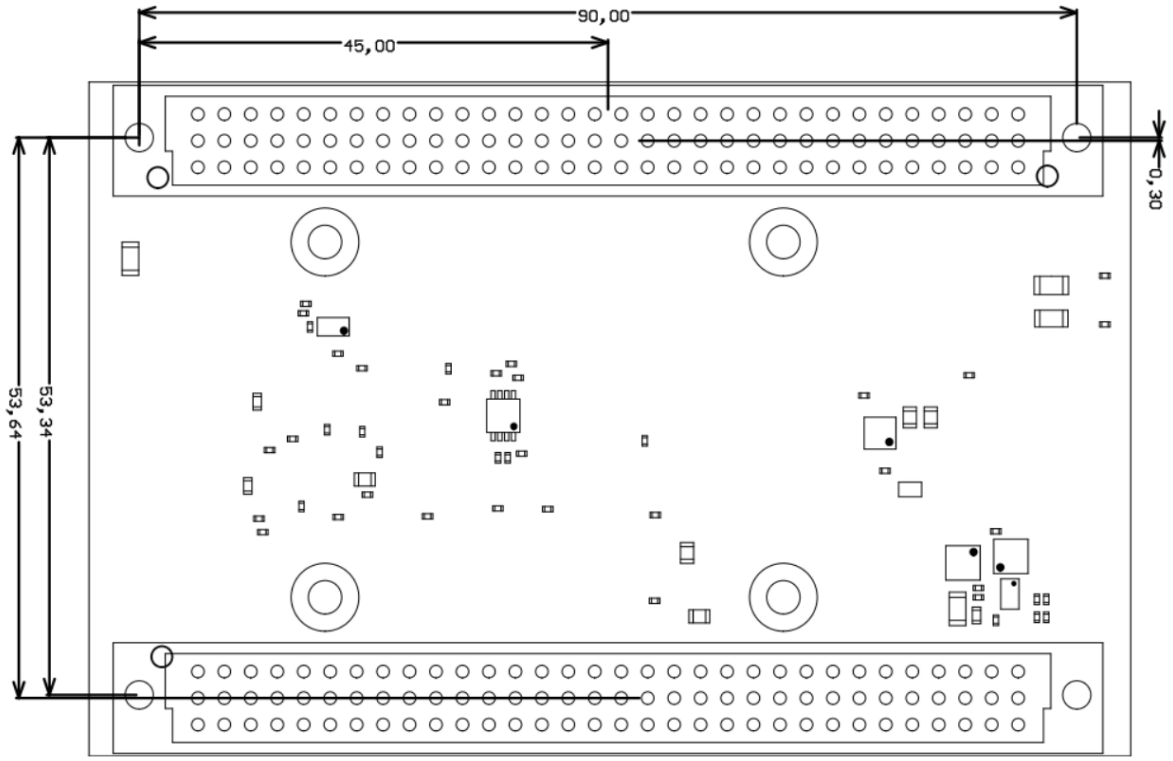


Physical Dimension

Operating Temperature Ranges

The carrier board itself is capable to be operated at industrial grade temperature range.

Please check the operating temperature range of the mounted modules which determines the relevant operating temperature range of the overall system.

Weight

42g - Plain board.

13g - 2 x VG96 connectors.

Revision History

Currently Offered Variants

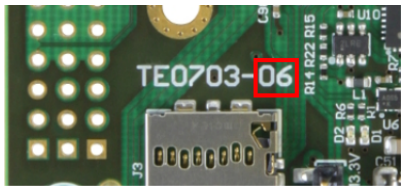
Trenz shop TE0728 overview page	
English page	German page

Trenz Electronic Shop Overview

Hardware Revision History

Date	Revision	Notes	PCN	Documents
2023-09-04	07	See Revision changes.		
2019-09-02	06	Added SD IO voltage selection jumper Further changes see PCN.	PCN-20190104	TE0703
2016-09-07	05	Added VCCIO Jumpers	PCN-20161122	TE0703-05
-	04	Corrected FTDI EEPROM connection	-	TE0703-04
-	03	Added VCCIO strapping resistors	-	
-	02	First series boards	-	
-	01	Prototypes	-	

Hardware revision number is printed on the PCB board next to the module model number separated by the dash.



Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• updated to REV07
2022-09-23	v.44	Mohsen Chamanbaz	• Changing in the dip-switches table because of updating of CPLD firmware (CPLD Firmware REV03)
2019-10-07	v.43	Martin Rohrmüller	• updated to REV06 • updated to TRM style 2.12

2018-06-13	v.29	Ali Naseri	• updating operating conditions
2017-02-07	v.28	John Hartfiel	• Add DIP setting description
2017-11-09	v.26	John Hartfiel	• add B2B connector section
2017-02-21	v.19	Jan Kumann	• New block diagram.
2017-02-02	v.16	Jan Kumann	• New board image with silk screen pin markings for VG96 connectors J1 and J2.
2016-12-22	v.14	Jan Kumann	• Block diagram added.
2016-12-08	v.10	Jan Kumann	• Document structure revised.
2016-12-05	v.5	John Hartfiel	• Corrected Boot Mode table.
2016-09-06	v.1	Jan Kumann, John Hartfiel	• Initial document.

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