TEI0022 TRM

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Overview

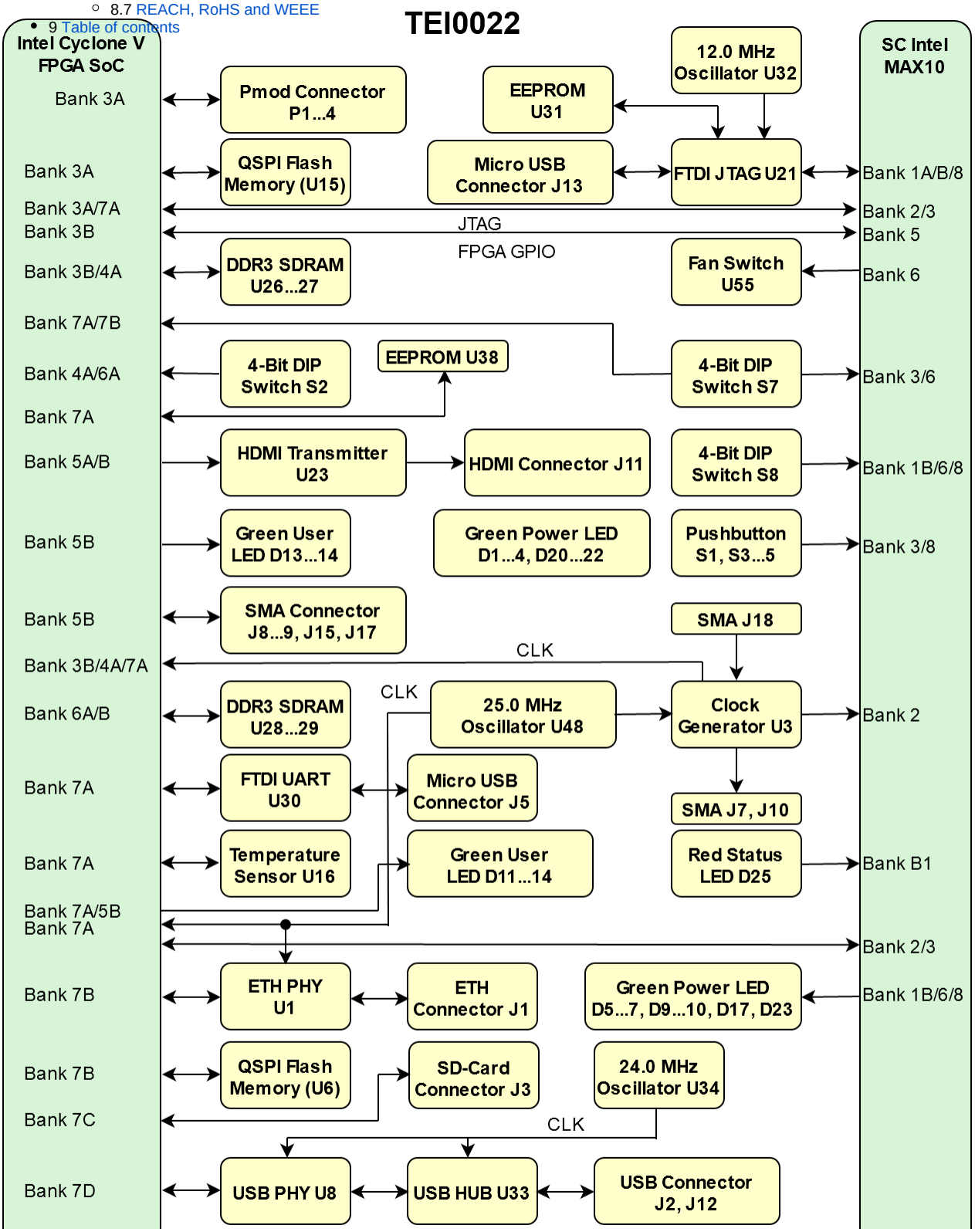
The Trenz Electronic TEI0022 is a SoC board based on Intel Cyclone V FPGA, an Ethernet PHY, one GByte DDR3 SDRAM per HPS and FPGA and one 32 MByte Quad SPI Flash memory for configuration and operation per HPS and FPGA, and powerful switching-mode power supplies for all on-board voltages.

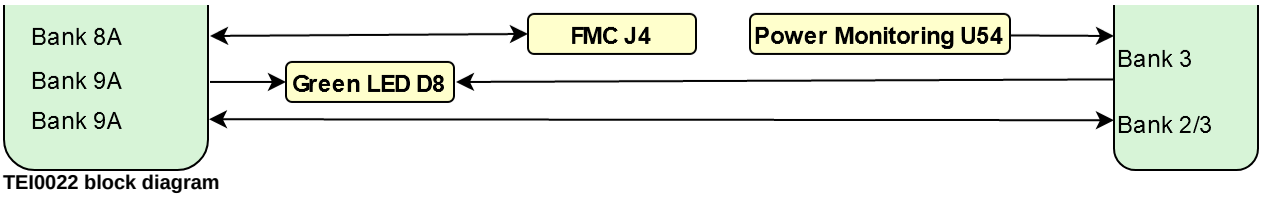
Refer to http://trenz.org/tei0022-info for the current online version of this manual and other available documentation.

Key Features

- **SoC FPGA**
  - Intel Cyclone V (5CSEMA5F31C8N)
  - Package: FBGA 896 pins
  - Speed Grade: 8
  - Temperature: Commercial (Tj = 0 °C to 85 °C)
- **RAM/Storage**
  - 1 GByte DDR3 SDRAM for HPS
  - 1 GByte DDR3 SDRAM for FPGA
  - 32 MByte SPI for HPS
  - 32 MByte SPI for FPGA
- **On Board**
  - up to 7 x SMA Connector
  - Temperature Sensor
  - Intel MAX10 for board management
- **Interface**
  - 1 PC FMC Connector
  - 4 x Pmod Connector
  - JTAG
  - UART via micro USB B Connector (for FPGA)
  - UART via micro USB B Connector (for HPS)
  - 4 x USB 2.0 Host
  - Ethernet via RJ45 Connector
  - SD Card
  - HDMI
- **Power**
  - 12 V Input supply voltage
- **Dimension**
  - 160 mm x 130 mm

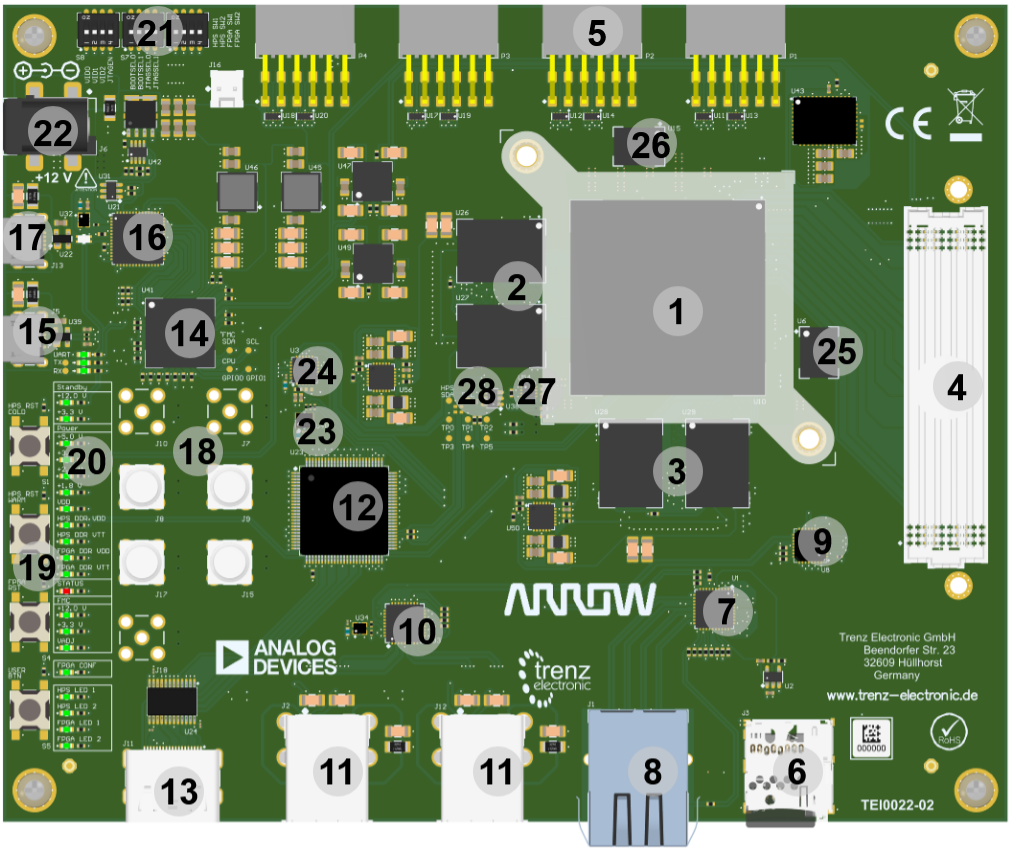
Block Diagram





TEI0022 block diagram

Main Components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ANALOG DEVICES
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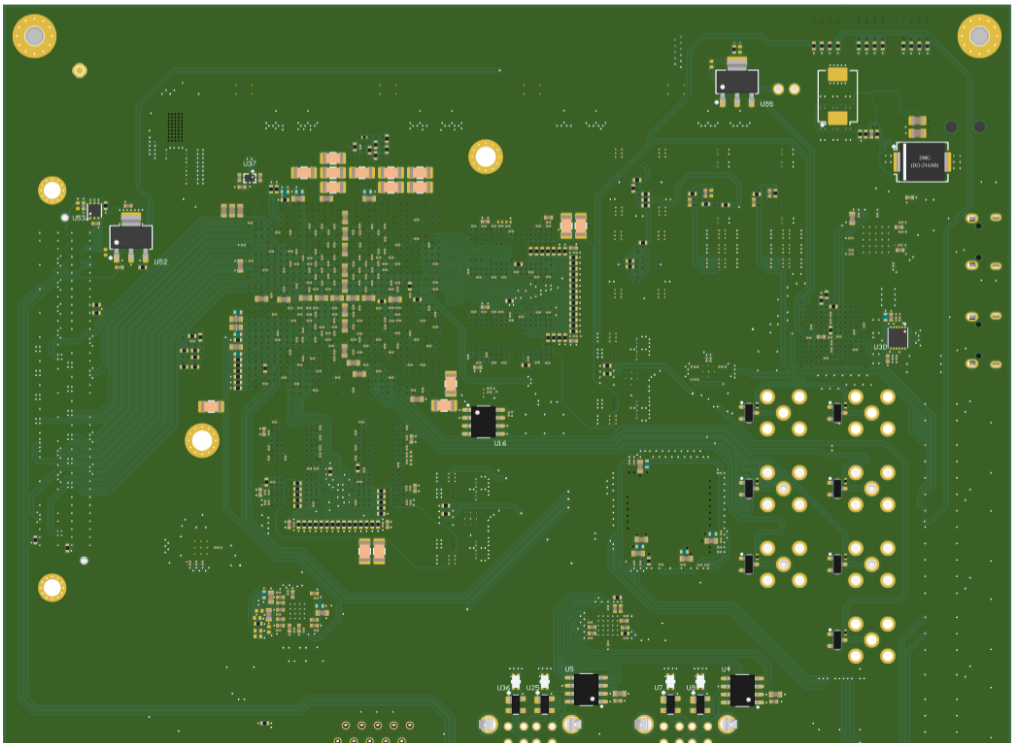
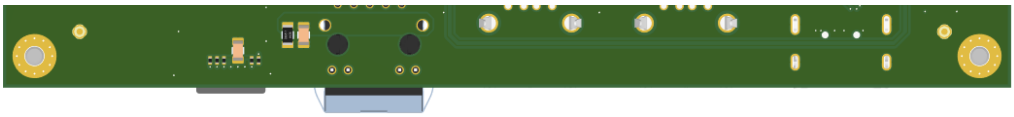




TEI0022 main components

1. Intel Cyclone V, U10
2. DDR3 SDRAM, U26...27
3. DDR3 SDRAM, U28...29
4. FMC, J4
5. Pmod, P1...4
6. SD Card Connector, J3
7. Ethernet PHY, U1
8. RJ45 Connector, J1
9. USB PHY, U8
10. USB HUB, U33
11. USB Connector, J2, J12
12. HDMI Transmitter, U23
13. HDMI Connector, J11
14. Intel MAX10, U41
15. Micro USB to UART Interface, J5, U30
16. USB to JTAG , U21
17. Micro USB JTAG and UART, J13
18. SMA Connector
19. Push Button, S1, S3...5
20. LED
21. 4-Bit DIP Switch, S2, S7...8
22. 12 V Power Jack, J6
23. Clock Generator, U48
24. Programmable Clock Generator, U3
25. QSPI - FPGA PS, U6
26. QSPI - FPGA PL, U15
27. Temperature Sensor, U16
28. EEPROM, U38

Initial Delivery State

Storage device name	Content	Notes
HPS SPI Flash (U6)	Not programmed	HPS Configuration
FPGA SPI Flash (U15)	Not programmed	FPGA Configuration
MAC EEPROM (U38)	MAC programmed, otherwise not programmed	Ethernet MAC
FTDI EEPROM (U31)	Programmed	FTDI Functionality
Programmable Clock Generator Si5338 (U3)	Programmed, CLK0 - 50M, CLK1 - 50M, CLK2 - 25M, CLK3 - 50M	--

Initial delivery state of programmable devices on the module

Configuration Signals

Boot Mode must be set using DIP Switch S7 on the module TEI0022. Please note that the DIP Switch is active low.

MODE Signal State	Boot Mode		Notes
	S7-1 (BOOTSEL0)	S7-2 (BOOTSEL1)	

FPGA	ON	ON	--
SD Card	ON	OFF	--
QSPI flash	OFF	OFF	--

Boot process.

Reset	Button	Notes
HPS cold reset	S1	--
HPS warm reset	S3	--
FPGA reset	S4	--

Reset process.

Signals, Interfaces and Pins

FMC LPC Connector

The FMC (FPGA Mezzanine Card) connector J4 with low pin count (LPC) provides as an ANSI/VITA 57.1 standard a modular interface to the Intel Cyclone V FPGA and exposes numerous of its I/O pins for use by other mezzanine modules and expansion cards.

The connector supports single ended (VCCIO: FMC_VADJ) and differential signaling as the I/O's are routed from the FPGA banks as LVDS-pairs to the FMC connector.

FMC Signal	Intel Cyclone V Direction	I/O Signal Count (Single Ended /Differential)	Voltage Level	Notes
LA0...1	RX	4 / 2	FMC_VADJ	Voltage level as visible in table Intel Cyclone V SoC bank voltages.
LA3, LA5, LA7, ..., LA33	RX	32 / 16	FMC_VADJ	Voltage level as visible in table Intel Cyclone V SoC bank voltages.
LA2, LA4, LA6, ..., LA32	TX	32 / 16	FMC_VADJ	Voltage level as visible in table Intel Cyclone V SoC bank voltages.
CLK0...1	RX	4 / 2	FMC_VADJ	Voltage level as visible in table Intel Cyclone V SoC bank voltages.

FMC connectors information

The FMC connector provides further interfaces like JTAG and I²C:

Interface	I/O Signal Count	Pin schematic Names / FMC Pins	Connected to	Notes

JTAG	5	FMC_TCK, Pin J4-D29 FMC_TMS, Pin J4-D33 FMC_TDI, Pin J4-D30 FMC_TDO, Pin J4-D31 FMC_TRST#, Pin J4-D34	Intel MAX10 U41, Bank 3	VCCIO: +3.3V
I2C	2	FMC_SCL, Pin J4-C30 FMC_SDA, Pin J4-C31	Intel MAX10 U41, Bank 3 and Intel Cyclone V U10, Bank 7A	I2C-lines pulled-up to +3.3V
Control Lines	2	FMC_PRSNT_M2C#, Pin J4-H2 (pulled-up to +3.3V) FMC_PG_C2M, Pin J4-D1 (pulled-up to +3.3V)	Intel MAX10 U41, Bank 3 and Intel Cyclone V U10, Bank 5B / 7C	'PG' = 'Power Good'-signal 'C2M' = carrier to (Mezzanine) module 'M2C' = (Mezzanine) module to carrier

FMC connector pin-outs of available interfaces

Several VCCIO voltages are available on the FMC connector to operate the I/O's on different voltage levels:

VCCIO Schematic Name	FMC Connector J4 Pins	Notes
+12.0V_FMC	C35/C37	extern 12 V power supply
+3.3V_FMC	D36/D38/D40/C39	3.3 V peripheral supply voltage
+3.3V	D32	3.3 V peripheral supply voltage
FMC_VADJ	H40/G39	adjustable FMC VCCIO voltage, supplied by DC-DC converter U43
FMC_VREF_A_M2C	H1	adjustable reference voltage

Available VCCIO voltages on FMC connector

Pmod Connector

The TEI0022 board offers four Pmod (2x6 pins, SMD) connectors which provides as a standard modular interface single ended I/O pins for use with extension modules.

Following table gives an overview of the Pmod connectors and the signals routed to the attached Intel Cyclone V (U10):

Pmod Connector P1 Pin	Signal Schematic Name	Connected to Intel Cyclone V, U10	Notes
1	P0_IO1	Pin AD9	--
2	P0_IO2	Pin AD11	--
3	P0_IO3	Pin AD12	--
4	P0_IO4	Pin AC12	--
7	P0_IO5	Pin AC9	--

8	P0_IO6	Pin AD10	--
9	P0_IO7	Pin AA12	--
10	P0_IO8	Pin AB12	--
Pmod Connector P2 Pin	**Signal Schematic Name**	**Connected to Intel Cyclone V, U10**	**Notes**
1	P1_IO1	Pin AG2	--
2	P1_IO2	Pin AF4	--
3	P1_IO3	Pin AF8	--
4	P1_IO4	Pin AD7	--
7	P1_IO5	Pin AG1	--
8	P1_IO6	Pin AF5	--
9	P1_IO7	Pin AE7	--
10	P1_IO8	Pin AE9	--
Pmod Connector P3 Pin	**Signal Schematic Name**	**Connected to Intel Cyclone V, U10**	**Notes**
1	P2_IO1	Pin AH5	--
2	P2_IO2	Pin AH3	--
3	P2_IO3	Pin AJ2	--
4	P2_IO4	Pin AG3	--
7	P2_IO5	Pin AG5	--
8	P2_IO6	Pin AH4	--
9	P2_IO7	Pin AH2	--
10	P2_IO8	Pin AJ1	--
Pmod Connector P4 Pin	**Signal Schematic Name**	**Connected to Intel Cyclone V, U10**	**Notes**
1	P3_IO1	Pin AE12	--
2	P3_IO2	Pin AF9	--
3	P3_IO3	Pin AG8	--
4	P3_IO4	Pin AG6	--
7	P3_IO5	Pin AE11	--
8	P3_IO6	Pin AF10	--
9	P3_IO7	Pin AG7	--
10	P3_IO8	Pin AF6	--

Pmod connectors pin description

SMA Connector

The TEI0022 board offers up to seven SMA connectors for trigger and clock input and output.

SMA Connector	Signal Schematic Names	Connected to	Notes

J7	SMA_CLK_OUT_p	Clock Generator U3, Pin 22	Assembly option
J10	SMA_CLK_OUT_n	Clock Generator U3, Pin 21	Assembly option
J8	TRIGGER_OUTPUT	Intel Cyclone V U10, Pin AE29	--
J9	TRIGGER_INPUT	Intel Cyclone V U10, Pin AA26	--
J15	EXT_CLK_INPUT	Intel Cyclone V U10, Pin Y26	--
J17	CLK_INPUT	Intel Cyclone V U10, Pin AD29	--
J18	SMA_CLK_IN	Clock Generator U3, Pin 1	Assembly option

SMA connectors

FAN Connector

The TEI0022 board offers a FAN connector for cooling the FPGA device. Depending on the assembly 5 V or 12 V are usable.

Connector	Signal Schematic Names	Connected to	Notes
2-Pin FAN Connector J16, 5 V or 12 V power supply depending on R270/271 with BTS4141N High Side Switch U55	FAN_EN, (High Side Switch U55, Pin 3)	Intel MAX10 U41, Pin D13	Intel Cyclone V cooling FAN

FAN connectors

Micro USB Connector (JTAG)

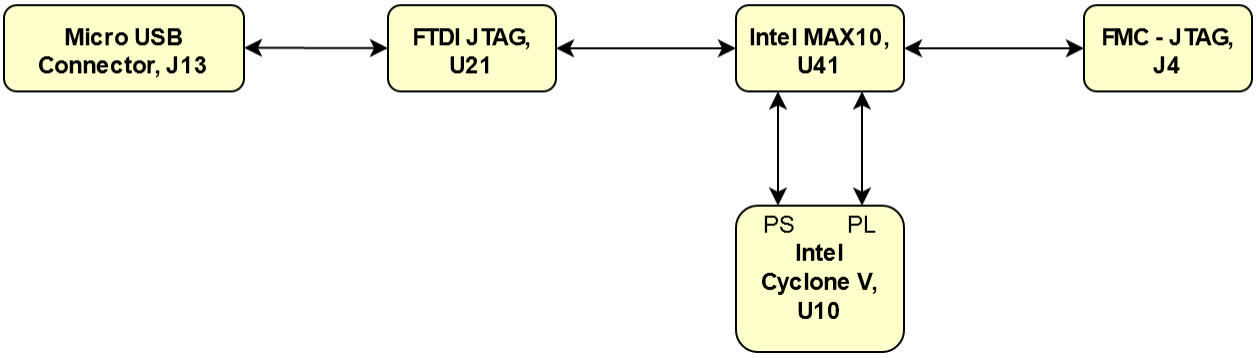
According to the JTAGEN and JTAGSEL[1..0] pins the management controller Intel MAX10 (U41), the Intel Cyclone V HPS (U10), the Intel Cyclone V FPGA (U10) or the FMC (J4) can be accessed via the micro USB B connector J13.

JTAG access is controlled by the DIP switches S7 and S8 on the module TEI0022. Please note that the DIP Switches are active low.

JTAG selection			JTAG Signal State	Note
S7-3 (JTAGSEL0)	**S7-4 (JTAGSEL1)**	**S8-4 (JTAGEN)**		
X	X	ON	Intel MAX10	--
ON	ON	OFF	Intel Cyclone V HPS	--
ON	OFF	OFF	Intel Cyclone V FPGA	--
OFF	ON	OFF	FMC	--

JTAG pins connection

TEI0022 - JTAG



TEI0022 JTAG

Micro USB Connector (UART)

A UART connection between the USB B connector J5 and the Intel Cyclone HPS U10 is possible via the FT234XD (U30) chip.

USB Connector

On the TEI0022 board there are up to four USB 2.0 Hi-Speed ports available (J2, J12).

HDMI Connector

The TEI0022 provides an HDMI Connector J11.

SD Card Connector

SD Card connector J3 is connected to the Intel Cyclone V U10.

RJ45 Connector

The board TEI0022 provides an ethernet interface via the RJ45 connector J1.

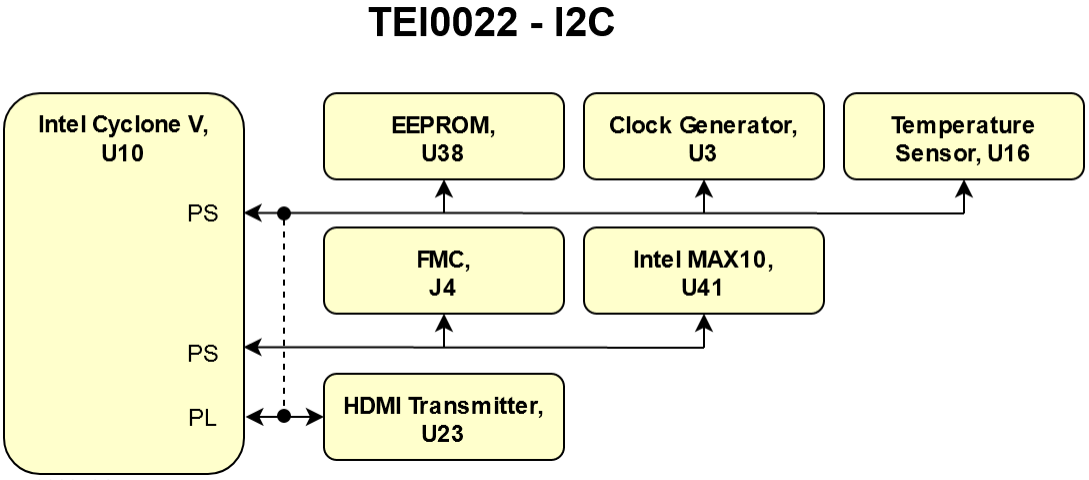
I2C

The TEI0022 provides three independent I2C busses. One bus is used to connect the FMC I2C with the Intel Cyclone V HPS. The second bus is used to connect the HDMI device to the Intel Cyclone V FPGA. The third bus is used to handle the other on-board I2C devices. Via assembly option, it is possible to connect bus two to bus three.

Bus	I2C Device	Designator	I2C Address	Schematic Names of I2C Bus Lines	Notes

HPS I2C	Temperature Sensor	U16	0x4A	HPS_I2C_SCL / HPS_I2C_SDA	3.3 V reference voltage
HPS I2C	Programmable Clock Generator	U3	0x70	HPS_I2C_SCL / HPS_I2C_SDA	3.3 V reference voltage
HPS I2C	EEPROM	U38	0x50	HPS_I2C_SCL / HPS_I2C_SDA	3.3 V reference voltage
HDMI I2C	HDMI	U23	0x72	HDMI_I2C_SCL / _I2C_SDA	3.3 V reference voltage
HPS FMC I2C	FMC	J4	0x50	FMC_SCL / FMC_SDA	3.3 V reference voltage

On-board peripherals' I2C-interfaces device slave addresses



TEI0022 I2C

On-board Peripherals

Chip/Interface	Designator	Notes
System Controller Intel MAX10	U41	--
Intel Cyclone V	U10	--
DDR3 SDRAM	U26...29	--
Gigabit Ethernet PHY	U1	--
High-Speed USB ULPI PHY	U8	--
4-Port USB 2.0 Hub	U33	--
HDMI Transmitter	U23	--
FTDI (JTAG)	U21	--
FTDI (UART)	U30	--
DIP-Switches	S2, S7...8	--
Buttons	S1, S3...5	--
On-Board LEDs	D1...15, D17...23, D25	--

Temperature Sensor	U16	--
QSPI	U6, U15	--
EEPROM	U31, U38	--
Clock Sources	U32, U34, U48	--
Programmable Clock Generator	U3	--
Power Monitoring	U54	--

On board peripherals

System Controller Intel MAX 10

The TEI0022 is equipped with an Intel MAX 10 (U41) which is the central system management unit where essential control signals are logically linked by the implemented logic of the FPGA firmware. This generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG are by-passed, forwarded and controlled by the System Controller. Other tasks of the System Controller are the monitoring of the power-on sequence and configuration of the Intel Cyclone V FPGA. The functionalities and configuration of the pins depend on its firmware.

Intel Cyclone V

The Intel Cyclone V device used at the TEI0022 board is a SoC with integrated ARM-based HPS. The 5CSEMA5F31C8N version delivers one hard memory controller, 80K logic elements in an FineLineBGA (FBGA) with 896 pins for the commercial temperature range of TJ = 0...85 °C with speed grade eight.

DDR3 SDRAM

The TEI0022 SoM has one GByte volatile DDR3 SDRAM memory per FPGA (U26, U27) and HPS (U28, U29) for storing user application code and data.

- Part number: IS43TR16256BL-125KBLI
- Supply voltage: 1.5 V
- Speed: TBD
- Temperature: TC = -40 °C up to 95 °C

Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY (U1) is provided with Analog Devices ADIN1300. The Ethernet PHY RGMII interface is connected to the Intel Cyclone V HPS. I/O voltage is fixed at 3.3 V. The reference clock input of the PHY is supplied from the on-board 25.0 MHz oscillator (U48).

Bank	Signal Name	Signal Description
7B	ETH_TXCK	RGMII Transmit Reference Clock
7B	ETH_TXD0	RGMII Transmit Data 0
7B	ETH_TXD1	RGMII Transmit Data 1
7B	ETH_TXD2	RGMII Transmit Data 2
7B	ETH_TXD3	RGMII Transmit Data 3
7B	ETH_TXCTL	RGMII Transmit Control

7B	ETH_RXCK	RGMII Receive Reference Clock
7B	ETH_RXD0	RGMII Receive Data 0
7B	ETH_RXD1	RGMII Receive Data 1
7B	ETH_RXD2	RGMII Receive Data 2
7B	ETH_RXD3	RGMII Receive Data 3
7B	ETH_RXCTL	RGMII Receive Control
7C	ETH_RST	Reset
7B	ETH_MDC	Management Data Clock
7B	ETH_MDIO	Management Data I/O
7B	PHY_INT	Interrupt

Ethernet PHY to HPS connections

High-Speed USB ULPI PHY

USB PHY (U8) is provided by USB3320C from Microchip. The ULPI interface is connected to the Intel Cyclone V HPS. I/O voltage is fixed at 3.3 V and PHY reference clock input is supplied from the on-board 24.0 MHz oscillator (U34).

PHY Pin	Connected to	Notes
ULPI	Intel Cyclone V HPS (U10)	--
REFCLK	24 MHz from on board oscillator (U34)	--
REFSEL[0..2]	High (3.3 V)	--
RESETB	Intel Cyclone V HPS (U10) and Intel MAX 10 (U41)	--
DP, DM	4-port USB 2.0 Hub (U33)	--
CPEN	Not Connected.	--
VBUS	Pull-up to 5 V.	--
ID	Not Connected.	--

USB PHY interface connections

4-Port USB 2.0 Hub

On the TEI0022 board there are up to four USB 2.0 Hi-Speed ports available (J2, J12). The USB 2.0 ports are provided by Microchip Cypress USB2514B 4-port USB 2.0 Hub controller (U33) which is connected to the USB PHY USB3320C (U8) connected to the Intel Cyclone V HPS via ULPI.

HDMI Transmitter

The TEI0022 board provides an HDMI interface routed to the Intel Cyclone FPGA (U10). The HDMI interface is created by the HDMI transmitter ADV7511 provided by Analog Devices. The HDMI transmitter is incorporated in conjunction with the HDMI protection circuit TI TPD12S016 for more signal robustness.

HDMI connector J11	Signal Schematic Name	Connected to	Notes
Pin 1, 3	HDMI_TX2_P / HDMI_TX2_N	HDMI transmitter, Pin 43, 42	also connected to HDMI protection circuit
Pin 4, 6	HDMI_TX1_P / HDMI_TX1_N	HDMI transmitter, Pin 40, 39	also connected to HDMI protection circuit
Pin 7, 9	HDMI_TX0_P / HDMI_TX0_N	HDMI transmitter, Pin 36, 35	also connected to HDMI protection circuit
Pin 10, 12	HDMI_TXC_P / HDMI_TXC_N	HDMI transmitter, Pin 33, 32	also connected to HDMI protection circuit
Pin 13	CEC_B	HDMI transmitter, Pin 48	HDMI CEC, wired through HDMI protection circuit
Pin 15	SCL_B	HDMI transmitter, Pin 53	HDMI I²C clock line, wired through HDMI protection circuit
Pin 16	SDA_B	HDMI transmitter, Pin 54	HDMI I²C data line, wired through HDMI protection circuit
Pin 19	HPD_B	HDMI transmitter, Pin 30	Hot Plug Detect, wired through HDMI protection circuit
Pin 18	5V_HDMI	HDMI protection circuit, Pin 13	5V supply voltage, wired through HDMI protection circuit

HDMI connector signals and pins

FTDI (JTAG)

Please refer to the section "Micro USB Connector (JTAG)".

FTDI (UART)

Please refer to the section "Micro USB Connector (UART)".

DIP-Switches

There are three 4-bit DIP-switches present on the TEI0022 board to configure options and set parameters. The following section describes the functionalities of the particular switches.

DIP-Switch S2

The table below describes the functionalities of the switches of DIP-switch S2 at their single positions:

DIP-switch S2	Position ON	Position OFF	Notes
S4-1	HPS_SW1 is low	HPS_SW1 is high	User switch
S4-2	HPS_SW2 is low	HPS_SW2 is high	User switch
S4-3	FPGA_SW1 is low	FPGA_SW1 is high	User switch
S4-4	FPGA_SW2 is low	FPGA_SW2 is high	User switch

DIP-switch S2 functionality description

DIP-Switch S7

The table below describes the functionalities of the switches of DIP-switch S7 at their single positions:

DIP-switch S7	Position ON	Position OFF	Notes
S7-1	HPS_SPI_SS /BOOTSEL0 is low	HPS_SPI_SS /BOOTSEL0 is high	Boot select (Firmware dependent)
S7-2	QSPI_CS/BOOTSEL1 is low	QSPI_CS/BOOTSEL1 is high	Boot select (Firmware dependent)
S7-3	JTAGSEL0 is low	JTAGSEL0 is high	JTAG select (Firmware dependent)
S7-4	JTAGSEL1 is low	JTAGSEL1 is high	JTAG select (Firmware dependent)

DIP-switch S7 functionality description

DIP-Switch S8

The table below describes the functionalities of the switches of DIP-switch S8 at their single positions:

DIP-switch S8	Position ON	Position OFF	Notes
S8-1	VID0_SW is low	VID0_SW is high	FMC_VADJ selection (Firmware dependent)
S8-2	VID1_SW is low	VID1_SW is high	FMC_VADJ selection (Firmware dependent)
S8-3	VID2_SW is low	VID2_SW is high	FMC_VADJ selection (Firmware dependent)
S8-4	JTAGEN is high	JTAGEN is low	JTAG select

DIP-switch S8 functionality description

Buttons

There are four buttons present on the TEI0022 board. The following section describes the functionalities of the particular buttons. The final functionality is set by the management Intel MAX10.

Button	Position ON	Position OFF	Notes
S1	HPS_RST#_SW is low	HPS_RST#_SW is high	Reset (cold) the Intel Cyclone V HPS (Firmware dependent)
S3	HPS_WARM_RST#_SW is low	HPS_WARM_RST#_SW is high	Reset (warm) the Intel Cyclone V HPS (Firmware dependent)
S4	FPGA_RST#_SW is low	FPGA_RST#_SW is high	Reset the Intel Cyclone V FPGA (Firmware dependent)
S5	USER_BTN_SW is low	USER_BTN_SW is high	User button (Firmware dependent)

Buttons functionality description

On-Board LEDs

The TEI0022 board is equipped with several LEDs to signal current states and activities. The functionality of the LEDs D11...14 are user LEDs. The LED D8 shows the Intel Cyclone V configuration progress. LEDs D15, D18...19 shows the UART connection and the other LEDs mentioned in the table are supply power status LEDs.

Designator	Color	Connected to	Active Level	Note
D11	Green	Intel Cyclone V HPS	H	User LED
D12	Green	Intel Cyclone V HPS	H	User LED
D13	Green	Intel Cyclone V FPGA	H	User LED
D14	Green	Intel Cyclone V FPGA	H	User LED
D8	Green	Intel Cyclone V FPGA, Intel MAX 10	L	Status: Configuration "Done"
D15	Green	FT234XD	L	UART
D18	Green	UART TX	L	UART
D19	Green	UART RX	L	UART
D21	Green	+12.0V	H	Status of +12.0V voltage rail
D1	Green	+12.0V_FMC	H	Status of +12. 0V_FMC voltage rail
D2	Green	+5.0V	H	Status of +5.0V voltage rail
D3	Green	+3.3V	H	Status of +3.3V voltage rail
D20	Green	+3.3V_MAX10	H	Status of +3. 3V_MAX10 voltage rail
D22	Green	+3.3V_FMC	H	Status of +3. 3V_FMC voltage rail
D4	Green	+2.5V	H	Status of +2.5V voltage rail
D5	Green	Intel MAX 10	H	Status of +1.8V voltage rail
D7	Green	Intel MAX 10	H	Status of VCC voltage rail
D9	Green	Intel MAX 10	H	Status of FMC_VADJ voltage rail
D6	Green	Intel MAX 10	H	Status of VDD_DDR_FPGA voltage rail
D23	Green	Intel MAX 10	H	Status of VDD_DDR_HPS voltage rail
D17	Green	Intel MAX 10	H	Status of VTT_DDR_FPGA voltage rail
D10	Green	Intel MAX 10	H	Status of VTT_DDR_HPS voltage rail
D25	Red	Intel MAX 10	H	Status

On-board LEDs

Temperature Sensor

The temperature sensor ADT7410 (U16) is implemented on the TEI0022 board.

Quad SPI Flash Memory

Two 256 Mbit (32 MByte) Quad SPI Flash Memory (Micron MT25QL256ABA8E12, U6, U15) are provided for FPGA and HPS configuration file storage. After configuration process completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA or the HPS allowing x1, x2 or x4 data bus widths to be used. The maximum data transfer rate depends on the bus width and clock frequency.

Quad SPI Flash memory U6 is connected to the HPS bank 7B and U15 to FPGA bank 3A.

Signal Name	QSPI Flash Memory U6 Pin	FPGA Pin
QSPI_CS/BOOTSEL1	S#, Pin C2	Bank 7B, Pin A18
QSPI_CLK	C, Pin B2	Bank 7B, Pin D19
QSPI_DATA0	DQ0, Pin D3	Bank 7B, Pin C20
QSPI_DATA1	DQ1, Pin D2	Bank 7B, Pin H18
QSPI_DATA2	DQ2, Pin C4	Bank 7B, Pin A19
QSPI_DATA3	DQ3, Pin D4	Bank 7B, Pin E19

HPS Quad SPI interface signals and connections

Signal Name	QSPI Flash Memory U15 Pin	FPGA Pin
nCSO	S#, Pin C2	Bank 3A, Pin AB8
AS_DCK	C, Pin B2	Bank 3A, Pin U7
AS_DATA0	DQ0, Pin D3	Bank 3A, Pin AE6
AS_DATA1	DQ1, Pin D2	Bank 3A, Pin AE5
AS_DATA2	DQ2, Pin C4	Bank 3A, Pin AE8
AS_DATA3	DQ3, Pin D4	Bank 3A, Pin AC7

FPGA Quad SPI interface signals and connections

EEPROM

The TEI0022 board contains two EEPROMs for configuration and general user purposes.

EEPROM Model	I2C Address	Designator	Memory Density	Purpose	Notes
24AA025E48T-I/OT	0x50	U38	2 KBit	Ethernet MAC	--
93AA56BT-I/OT	-	U31	2 KBit	JTAG Configuration	--

On-board configuration EEPROMs overview

Clock Sources

The board has following reference clocking sources provided by on-board oscillators:

Clock Source	Frequency	Signal Schematic Name	Clock Destination	Notes
U48, SiT8208AI	25.0 MHz	CLK_25MHz_R	Si5338A PLL U3, Pin 3 (IN3)	--
		HPS_CLK1_25MHz	HPS Bank 7A U10, Pin D25	--
		ETH_XTAL_IN	ETH PHY U1, Pin 9	--
U32, SiT8208AI	12.0 MHz	OSCI	FT2232H U21, Pin 3	--
U34, SiT8008BI	24.0 MHz	USB_CLK24_HUB	USB Hub U33, Pin 33	--
		USB_CLK24_PHY	USB PHY U8, Pin 26	--

Reference clock signals

Programmable Clock Generator

There is a Silicon Labs I^2C programmable quad PLL clock generator on-board (Si5338A, U3) to generate various reference clocks for the module. The I^2C Address is 0x70.

Si5338A Pin	Signal	Connected to	Direction	Default frequency	Standard	Notes
IN1	SMA_CLK_IN	SMA J18, Pin 1	Input	--	--	Assembly option dependent
IN2	SMA_CLK_IN	SMA J18, Pin 1	Input	--	--	Assembly option dependent
IN3	CLK_25MHz_R	U48, Pin 3	Input	25MHz	--	Reference input clock
IN4	--	GND	Input	--	--	I^2C slave device address LSB
IN5	--	Not Connected	Input	--	--	Not used
IN6	--	GND	Input	--	--	Not used
SCL	HPS_I2C_SCL	Cyclone V Bank 7A/Pin H23	Input	--	--	I²C interface
SDA	HPS_I2C_SDA	Cyclone V Bank 7A/Pin A25	Input / Output	--	--	I²C interface
CLK0A/B	SMA_CLK_OUT_p/n	SMA, J7/J10	Output	50MHz	LVDS 3.3V	Assembly option dependent
CLK1A/B	CLK_B3B_p/n	Cyclone V FPGA Bank 3B/Pin AF14/AF15	Output	50MHz	LVDS 1.8V	--
CLK2A	CLK_MAX10	MAX10 Bank 2/Pin H6	Output	25MHz	CMOS 3.3V	--

CLK2B	HPS_CLK2	Cyclone V HPS Bank 7A /Pin F25	Output	25MHz	CMOS 3.3V	--
CLK3A/B	CLK_B4A_p/n	Cyclone V FPGA Bank 4A/Pin AA16 /AB17	Output	50MHz	LVDS 1.8V	--

Programmable quad PLL clock generator inputs and outputs

Power Monitoring

The TEI0022 uses a precision supply monitor (U54) for three voltages. Therefore, if one of the voltages browns out it should be realized and handled.

Power and Power-On Sequence

Power Supply

The maximum power consumption of this board mainly depends on the design which is running on the FPGA. Intel provides power estimator excel sheets to calculate power consumption.

Power Consumption

Power Input Pin	Typical Current
+12.0V_IN	TBD*

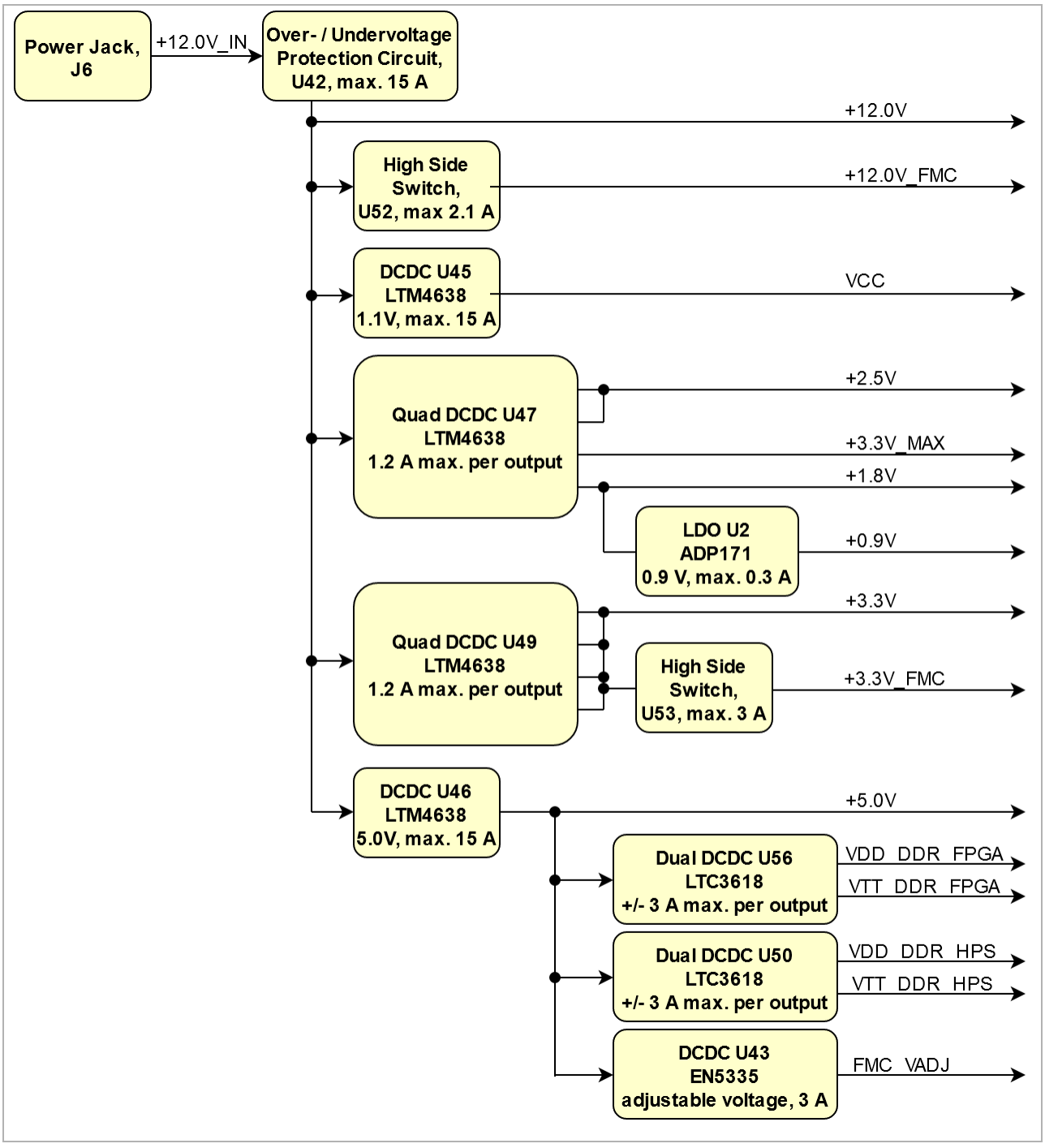
Power Consumption

* TBD - To Be Determined

Power Distribution Dependencies

All on-board voltages of the TEI0022 are generated out of the extern applied 12 V power supply.

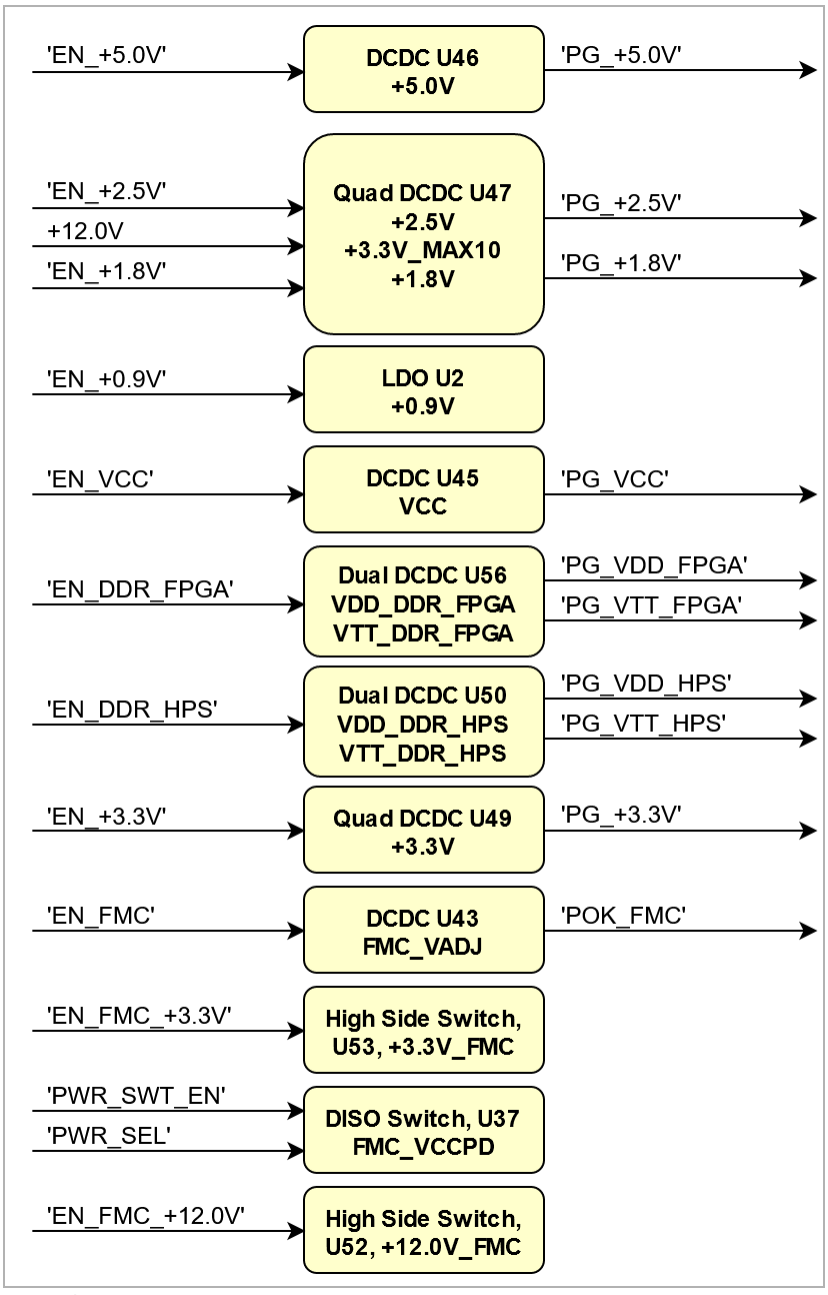
There are following dependencies how the initial 12V power supply is distributed to the on-board DC-DC converters, which power up further DCDC converters and the particular on-board voltages:



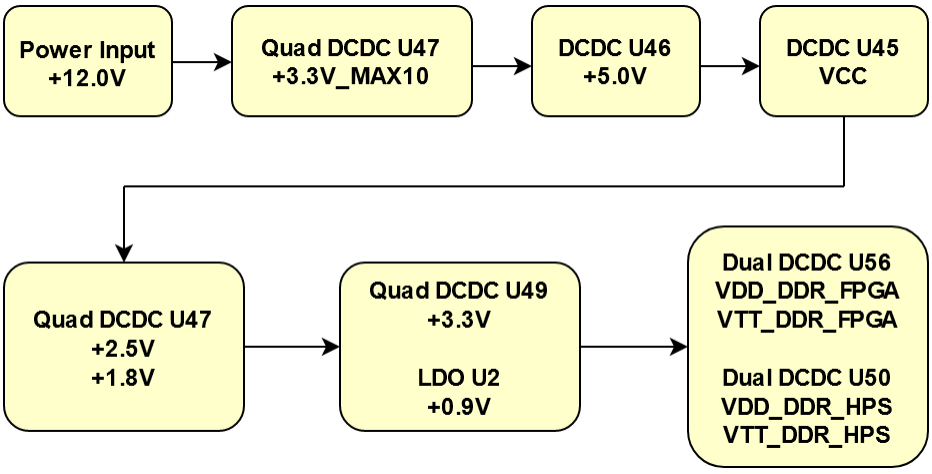
Power Distribution

Power-On Sequence

The following figures delivers the power-on sequence information. The figure Power Sequency shows the connections between the power devices and its management. The figure Suggested Power Sequency shows the recommended firmware power-on sequence. For more information about firmware depended power-on sequencing see TEI0022 Intel MAX 10 Power mangement.



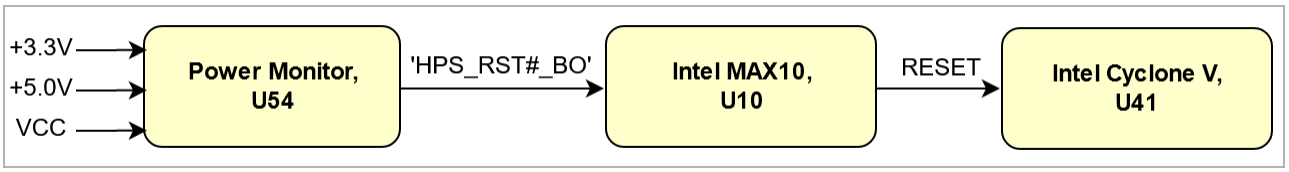
Power Sequency



Suggested Power Sequency

Voltage Monitor Circuit

The voltages +3.3V, +5.0V, and VCC are monitored by the voltage monitor circuit LTC2911 (U54), which generates a reset signal at power-on. A manual reset is also possible as described in the reset table.



Voltage Monitor Circuit

Bank Voltages

Bank	Schematic Name	Voltage	Notes
Bank 3A	+3.3V	+3.3 V	--
Bank 3B	VDD_DDR_FPGA	+1.5 V	--
Bank 4A	VDD_DDR_FPGA	+1.5 V	--
Bank 5A	+3.3V	+3.3 V	--
Bank 5B	+3.3V	+3.3 V	--
Bank 6A	VDD_DDR_HPS	+1.5 V	--
Bank 6B	VDD_DDR_HPS	+1.5 V	--
Bank 7A	+3.3V	+3.3 V	--
Bank 7B	+3.3V	+3.3 V	--
Bank 7C	+3.3V	+3.3 V	--
Bank 7D	+3.3V	+3.3 V	--
Bank 8A	FMC_VADJ	+3.3 V, +2.5 V, +1.8 V, +1.25 V, +1.2 V	Adjustable voltage (+0.8 V is not usable at the Intel Cyclone V)

Bank 9A	+3.3V	+3.3 V	--

Intel Cyclone V SoC bank voltages.

Technical Specifications

Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
+12.0V_IN	Input Voltage	-25	25	V

PS absolute maximum ratings

Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

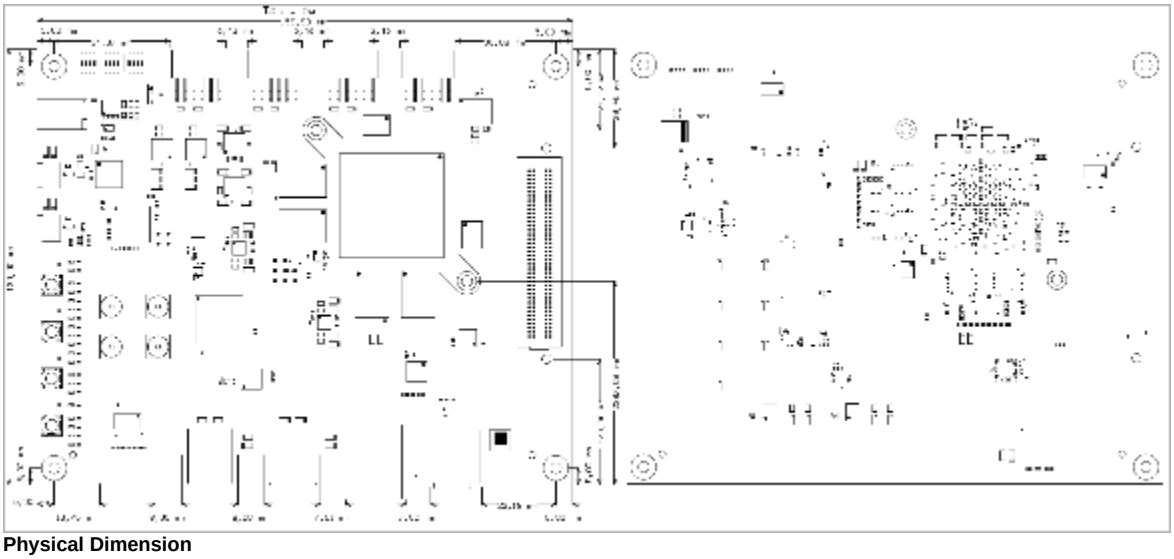
Parameter	Min	Max	Units	Reference Document
+12.0V_IN	10.5	13	V	Input power protection U42

Recommended operating conditions.

Physical Dimensions

- Module size: 160 mm × 130 mm. Please download the assembly diagram for exact numbers.

PCB thickness: 1.9 mm.



Physical Dimension

Currently Offered Variants

Trenz shop TEI0022 overview page	
English page	German page

Trenz Electronic Shop Overview

Revision History

Hardware Revision History

Date	Revision	Changes	Documentation Link
-	03	Refer to the "Revision_Changes" schematic page	
-	02	Refer to the "Revision_Changes" schematic page	
-	01	First Production Release	

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

Board hardware revision number.

Document Change History

Date	Revision	Contributor	Description
Error rendering macro 'page-info' Ambiguous	**Error rendering macro 'page-info'** Ambiguous	**Error rendering macro 'page-info'** Ambiguous	• add default frequency and IO Standard to 'Programmable Clock Generator' • Style update

method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interfac

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e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	e com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

2022-06-15	v.55	Thomas Dück	• typo correction
2020-11-03	v.52	ED	• Update TRM to REV03
2020-06-03	v.48	TD	• Chapter 'Power-On Sequence' updated
2020-02-26	v.47	ED	• Update TRM to REV02
--	all	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null,	• Initial Document

class java. lang. String, class com. atlassian . confluen ce. pages. Page] due to overlapp ing prototyp es between : [interfac e com. atlassian . confluen ce.user. Conflue nceUser , class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb

		ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	

Document change history.

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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]