

CR00140 SC CPLD MAX10

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Overview

CR00140 SC CPLD design for MAX10 with designator U25: 10M08SAU169C8G.

Feature Summary

- Receiving, levelshifting and forwarding of
 - control,
 - sensor, measurement and
 - status signals
- security logic
- Push Buttons
- USR LED

Firmware Revision and supported PCB Revision

See Document Change History.

Product Specification

Port Description

VHDL Port name	Direction	SC CPLD Pin	CPLD Bank	Connected to	Function	Notes
A0_P	in	J8	3	J9-14	PWM signal phase B, low	-
A0_N	in	K8	3	J9-16	PWM signal phase D, high	-
A1_P	in	M13	3	J9-20	PWM signal phase A, low	-
A1_N	in	M12	3	J9-22	PWM signal phase C, high	-
A2_P	in	M9	3	J9-26	PWM signal phase D, low	-
A2_N	in	M8	3	J9-28	PWM signal phase C, low	-
A3_P	in	N8	3	J9-32	PWM signal phase B, high	-
A3_N	in	N7	3	J9-34	PWM signal phase A, high	-
A4_P	out	M7	3	J9-38	current measurement phase B	-
A4_N	out	N6	3	J9-40	push button S2 signal	-
A5_P	out	K5	3	J9-44	motor disable signal	disabled when high
A5_N		J5	3	J9-46	CPLD - CRUVI communication	currently not used
B0_P		N5	3	J9-15	CPLD - CRUVI communication	currently not used
B0_N	in	N4	3	J9-17	LED D2 signal	active high
B1_P		J7	3	J9-21	CPLD - CRUVI communication	PWM enable
B1_N	in	K7	3	J9-23	clock input for ADCs	5-20 MHz
B2_P	out	L11	3	J9-27	Encoder/Sensor signal A	-
B2_N	out	M11	3	J9-29	Encoder/Sensor signal B	-
B3_P	out	L10	3	J9-33	Encoder/Sensor signal I	-
B3_N	out	M10	3	J9-35	Back EMF signal phase B	-
B4_P	out	J6	3	J9-398	Back EMF signal phase C	-
B4_N	out	K6	3	J9-41	Back EMF signal phase A	-
B5_P	out	L5	3	J9-45	current measurement phase A	-
B5_N	out	L4	3	J9-47	voltage measurement DC_LINK	-
HSIO		N9	3	J9-2	CPLD - CRUVI I/O communication	currently not used
HSO		N10	3	J9-6		
RESET		M5	3	J9-8		
HSI		N12	3	J9-10		
TDI		F5	1B	J9-51, J10-9	JTAG / user IO CPLD firmware dependent	JTAG pinsharing currently not enabled
TDO		F6	1B	J9-53, J10-3	JTAG / user IO CPLD firmware dependent	
TMS		G1	1B	J9-55, J10-5	JTAG / user IO CPLD firmware dependent	
JTAGEN		E5	1B	J9-57	JTAG enable CPLD firmware dependent	
TCK		G2	1B	J9-59, J10-1	JTAG / user IO CPLD firmware dependent	
SMB_ALERT		K2	2	J9-3	CPLD - CRUVI I/O communication	currently not used
SMB_SDA		H5	2	J9-5		
SMB_SCL		H4	2	J9-7		
REFCLK		M2	2	J9-11		
BUTTON1	in	C10	8	S2	User button forwarded to CRUVI	activ low

BUTTON2	in	B10	8	S1	Motor control enable/disable	activ low
ENC_A	in	A10	8	U13-13	Sensor/Encoder input channel A	-
ENC_B	in	A9	8	U13-12	Sensor/Encoder input channel B	-
ENC_I	in	A11	8	U13-14	Sensor/Encoder input channel I	-
LED0	out	D6	8	D2	User LED forwarded from CRUVI	active high
LED1	out	B2	8	D1	Status LED	blinking motor control aktiv, static on system ok and motor control disabled
M_BEMF_B_D	in	B5	8	U15-13	Back EMF signal phase B	-
M_BEMF_C_D	in	A5	8	U15-12	Back EMF signal phase C	-
M_BEMF_A_D	in	A4	8	U15-14	Back EMF signal phase A	-
M_PWM_AH	out	F1	1A	U8-2	Phase A half bridge high (DC_LINK) side driver signal	-
M_PWM_AL	out	E3	1A	U8-3	Phase A half bridge low (PGND) side driver signal	-
M_PWM_BH	out	E1	1A	U9-2	Phase B half bridge high (DC_LINK)side driver signal	-
M_PWM_BL	out	D1	1A	U9-3	Phase B half bridge low (PGND) side driver signal	-
M_PWM_CH	out	E4	1A	U10-2	Phase C half bridge high (DC_LINK)side driver signal	-
M_PWM_CL	out	C1	1A	U10-3	Phase C half bridge low (PGND) side driver signal	-
M_PWM_DH	out	C2	1A	U11-2	Phase D half bridge high (DC_LINK) side driver signal	-
M_PWM_DL	out	B1	1A	U11-3	Phase D half bridge low (PGND) side driver signal	-
SD_IA	in	E6	8	U3-6	Current measurement phase A	-
SCLK_A	out	B3	8	U3-7, U5-7	Clock for ADC for current measurement phase A and B	(5-20 MHz)
SD_V	in	B4	8	U7-6	Voltage measurement DC_LINK	-
SD_IB	in	A2	8	U5-6	Current measurement phase B	-
SCLK_V_A	out	A3	8	U7-7	Clock for ADC for voltage measurement DC_LINK	(5-20 MHz)
M_DISABLE_D_D	out	J1	2	U11-5	Halfe bridge disable phase D	disabled when high, pull up connected, weak pull up enabled
M_DISABLE_A_D	out	M1	2	U8-5	Halfe bridge disable phase A	disabled when high, pull up connected, weak pull up enabled
M_DISABLE_B_D	out	L2	2	U9-5	Halfe bridge disable phase B	disabled when high, pull up connected, weak pull up enabled
M_DISABLE_C_D	out	K1	2	U10-5	Halfe bridge disable phase C	disabled when high, pull up connected, weak pull up enabled
REFCLK		M2	2	J9-11	-	currently not used
RST		M3	2	J10-6	-	currently not used (CPLD RESET)
UART_RX		N2	2	J10-7	-	currently not used/implemented (UART)
UART_TX		N3	2	J10-8		
CLK_25MHZ	in	H6	2	U26-3	Clock input for accurate 25 Mhz.	currently not used

On-board LEDs

Motor driver PWM signals

CRUVI interface signals are utilized to drive the half bridge PWM motor driver signals. They are logical connected to prevent driving the high and low simultaneously:

```

M_PWM_AH <= '1' when ((A3_N='1') and (A1_P = '0')) else '0';
M_PWM_AL <= '1' when ((A1_P='1') and (A3_N = '0')) else '0';

M_PWM_BH <= '1' when ((A3_P='1') and (A0_P = '0')) else '0';
M_PWM_BL <= '1' when ((A0_P='1') and (A3_P = '0')) else '0';

M_PWM_CH <= '1' when ((A1_N='1') and (A2_N = '0')) else '0';
M_PWM_CL <= '1' when ((A2_N='1') and (A1_N = '0')) else '0';

M_PWM_DH <= '1' when ((A0_N='1') and (A2_P = '0')) else '0';
M_PWM_DL <= '1' when ((A2_P='1') and (A0_N = '0')) else '0';

```

Motor disable

The M_DISABLE signal set via push button S1 is used to disable all 4 motor drivers. This signal is logical or to the PWM enable signal from B1_P on the CRUVI connector.

```
M_DISABLE_OUT <= M_DISABLE or not B1_P;
```

```

M_DISABLE_A_D <= M_DISABLE_OUT;
M_DISABLE_B_D <= M_DISABLE_OUT;
M_DISABLE_C_D <= M_DISABLE_OUT;
M_DISABLE_D_D <= M_DISABLE_OUT;

```

The motor disable signal is also forwarded to the CRUVI interface:
A5_P <= M_DISABLE;

Sensor/Encoder, Back EMF

Sensor signals are forwarded to the CRUVI interface:

```

B2_P <= ENC_A;
B2_N <= ENC_B;
B3_P <= ENC_I;

B3_N <= M_BEMF_B_D;
B4_N <= M_BEMF_A_D;
B4_P <= M_BEMF_C_D;

```

Current and voltage measurement

Data signals from the 3 ADCs are forwarded to the CRUVI interface:

```

B5_N <= SD_V;
B5_P <= SD_IA;
A4_P <= SD_IB;

```

The corresponding clock signals are derived from the CRUVI interface signal B1_N:

```

SCLK_V_A <= B1_N;
SCLK_A <= B1_N;

```

Button

Motor disable button

S1 is utilized to switch the motor control on/off. The button is debounced. On press it switches the state of M_DISABLE signal and sets the corresponding LED status.

User Button

User button S2 is forwarded to the CRUVI interface signal A4_N:
A4_N <= BUTTON1;

LEDs

Status LED

The LED D1 is utilized for board status information in the following way:

Sequenz		Description
ON	LED ON	All OK, motor control disabled
*****	continuous blinking	All OK, motor control enabled
*oooooooo to *****o	1 to 7 times blinking with a break	currently not used

Status LED description

USR LED

User LED D2 is controlled via the CRUVI signal B0_N:
LED0 <= B0_N;

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Revision Changes

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV01	REV01, REV02	<div>Error rendering macro 'page-info' Ambiguou s method overloadin g for method jdk. proxy241. \$Proxy349 6#hasCon</div>	initial version

Error rendering macro 'page-info'

Ambiguous method
overloading for method jdk.
proxy241.\$Proxy3496#hasCon
tentLevelPermission. Cannot
resolve which method to
invoke for [null, class java.lang.
String, class com.atlassian.
confluence.pages.Page] due
to overlapping prototypes
between: [interface com.
atlassian.confluence.user.
ConfluenceUser, class java.
lang.String, class com.
atlassian.confluence.core.
ContentEntityObject] [interface
com.atlassian.user.User, class
java.lang.String, class com.
atlassian.confluence.core.
ContentEntityObject]

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atlassian.confluence.user.
ConfluenceUser, class java.
lang.String, class com.
atlassian.confluence.core.
ContentEntityObject] [interface
com.atlassian.user.User, class
java.lang.String, class com.
atlassian.confluence.core.
ContentEntityObject]

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