TEI0006 Intel MAX 10

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Overview

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Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Pullup/Down	Bank Power	Description
AIN		D2	--	3.3V	B2B connector J2-115 / currently_not_used
AIN0		D1	--	3.3V	B2B connector J2-116 / currently_not_used
AIN1		F1	--	3.3V	B2B connector J2-117 / currently_not_used
AIN2		E1	--	3.3V	B2B connector J2-121 / currently_not_used
AIN3		E4	--	3.3V	B2B connector J2-118 / currently_not_used
AIN4		C2	--	3.3V	B2B connector J2-128 / currently_not_used
AIN5		E3	--	3.3V	B2B connector J2-123 / currently_not_used

AIN6		C1	--	3.3V	B2B connector J2-122 / currently_not_used
AIN7		B1	--	3.3V	B2B connector J2-130 / currently_not_used
CONF_DONE	in	N7	--	1.8VIO	Configuration done pin, Intel Cyclone 10 GX
DATA0	in	N5	--	1.8VIO	Intel Cyclone 10 GX LED_FP_4
DCLK	in	M4	--	1.8VIO	Dedicated configuration clock pin, Intel Cyclone 10 GX / currently_not_used
DEV_CLRN	out	J5	--	1.8VIO	used as I/O, Intel Cyclone 10 GX B2B J2-154 (TEIB0006 LED2)
DIS_GROUP1	out	K12	--	3.3V	Fast Discharging
DIS_GROUP2	out	K10	--	3.3V	Fast Discharging
DIS_GROUP3	out	J9	--	3.3V	Fast Discharging
DIS_GROUP4	out	J12	--	3.3V	Fast Discharging
EN_0V9	out	E9	--	3.3V	Power enable signal 0.9V
EN_0V95	out	J10	--	3.3V	Power enable signal 0.95V
EN_1V8	out	D9	--	3.3V	Power enable signal 1.8V
EN_1V8VIO	out	L12	--	3.3V	Power enable signal 1.8VIO
EN_1V35	out	D12	--	3.3V	Power enable signal 1.35V
EN_VTT	out	C11	--	3.3V	Power enable signal VTT
ETH1_CLK125	out	N3	--	1.8VIO	currently_not_used
ETH1_RXDV	out	J2	--	1.8VIO	currently_not_used
F_TCK	out	N2	--	1.8VIO	JTAG, Intel Cyclone 10 GX
F_TDI	out	M2	--	1.8VIO	JTAG, Intel Cyclone 10 GX
F_TDO	in	M3	--	1.8VIO	JTAG, Intel Cyclone 10 GX
F_TMS	out	K1	--	1.8VIO	JTAG, Intel Cyclone 10 GX
I2C1_SCL	inout	D11	--	3.3V	currently_not_used
I2C1_SDA	inout	C13	--	3.3V	currently_not_used
I2C_18_RST	out	H6	--	1.8VIO	currently_not_used
I2C_SCL	inout	K2	--	1.8VIO	Clock signal for I2C interface

I2C_SDA	inout	L2	--	1.8VIO	Data signal for I2C interface
INIT_DONE	out	L4	--	1.8VIO	used as I/O, Intel Cyclone 10 GX B2B J2-154 (TEIB0006 USER_BTN2)
LED_FP_1	out	B13	--	3.3V	red led D1, status led
LED_FP_2	out	B11	--	3.3V	user defined, green led D2
LED_FP_3	out	A12	--	3.3V	user defined, green led D3
LED_FP_4	out	B12	--	3.3V	user defined, green led D4
M10_CLK	in	G9	--	3.3V	Clock input signal, 25 MHz
M10_IO1	out	K5	--	1.8VIO	UART Intel Cyclone 10 GX
M10_IO2	in	N6	--	1.8VIO	UART Intel Cyclone 10 GX
M10_IO3	in	J6	--	1.8VIO	Intel Cyclone 10 GX LED_FP_2
M10_IO4	in	K6	--	1.8VIO	Intel Cyclone 10 GX LED_FP_3
MAX_IO1	out	E8	--	3.3V	B2B connector J2-134 / currently_not_used
MAX_IO2	out	A4	--	3.3V	B2B connector J2-136 / currently_not_used
MAX_IO3	out	D8	--	3.3V	B2B connector J2-140 / currently_not_used
MAX_IO4	in	B4	--	3.3V	B2B connector J2-142 / currently_not_used
MAX_IO5	out	A6	--	3.3V	B2B connector J2-146 / Led "LED1" from carrier board TEIB0006
MAX_IO6	out	A3	--	3.3V	B2B connector J2-148 / Led "LED2" from carrier board TEIB0006
MAX_IO7	in	C9	--	3.3V	B2B connector J2-152 / User button "USER_BTN1" from carrier board TEIB0006
MAX_IO8	in	B3	--	3.3V	B2B connector J2-154 / User button "USER_BTN2" from carrier board TEIB0006
MAX_IO9	out	E6	--	3.3V	B2B connector J2-127 / currently_not_used

MAX_IO10	out	D6	--	3.3V	B2B connector J2-129 / currently_not_used
MAX_IO11	out	B5	--	3.3V	B2B connector J2-133 / currently_not_used
MAX_IO12	out	B6	--	3.3V	B2B connector J2-135 / currently_not_used
MAX_IO13	out	A7	--	3.3V	B2B connector J2-139 / currently_not_used
MAX_IO14	out	A8	--	3.3V	B2B connector J2-141 / currently_not_used
MAX_IO15	out	A9	--	3.3V	B2B connector J2-145 / currently_not_used
MAX_IO16	in	B2	--	3.3V	B2B connector J2-98 / currently_not_used
MAX_IO17	out	A10	--	3.3V	B2B connector J2-151 / UART TEIB0006
MAX_IO18	in	B10	--	3.3V	B2B connector J2-153 / UART TEIB0006
MAX_IO19	out	A11	--	3.3V	B2B connector J2-74 / Power enable signal 3.3V for carrier board TEIB0006 EN_3V3MB
MAX_IO20	in	C10	Pullup	3.3V	B2B connector J2-76 / Power good signal 3.3V for carrier board TEIB0006 PG_MB_3.3V
MAX_IO22	in	A5	Pullup	3.3V	B2B connector J2-82 / Power good signal 1.8V for carrier board TEIB0006 PG_MB_1.8V
MAX_IO23	out	H9	--	3.3V	B2B connector J2-86 / Power enable signal 1.8V for carrier board TEIB0006 EN_1V8MB
MAX_IO25	in	H13	--	3.3V	B2B connector J2-92 / currently_not_used
MAX_IO26	out	H8	--	3.3V	B2B connector J2-94 / currently_not_used
MSEL0	out	M7	--	1.8VIO	configuration mode selection, Intel Cyclone 10 GX

MSEL1	out	M9	--	1.8VIO	configuration mode selection, Intel Cyclone 10 GX
NCONFIG	out	M8	--	1.8VIO	FPGA configuration pin, Intel Cyclone 10 GX
NSTATUS	in	M5	--	1.8VIO	FPGA configuration pin, Intel Cyclone 10 GX
PG_0V9	in	E10	--	3.3V	Power Good signal 0.9V, U4
PG_0V95	in	H10	--	3.3V	Power Good signal 0.95V, U7
PG_1V8	in	F8	--	3.3V	Power Good signal 1.8V, U5
PG_1V8VIO	in	K11	--	3.3V	Power Good signal 1.8VIO, U6
PG_1V35	in	E12	--	3.3V	Power Good signal 1.35V, U8
PG_VADJ	in	G10	--	3.3V	Power Good signal VADJ, U11
PHY1_33LED1	out	F10	--	3.3V	B2B connector J2-67 / green led from RJ45-connector on carrier board TEIB0006
PHY1_33LED2	out	F9	--	3.3V	B2B connector J2-69 / yellow led from RJ45-connector on carrier board TEIB0006
PHY1_LED1	in	J1	--	1.8VIO	led output pin from ethernet phy U2
PHY1_LED2	in	H5	--	1.8VIO	led output pin from ethernet phy U2
PLL_RST	out	L3	--	1.8VIO	Device reset for porgrammable oscillator SI5345A, U14
TCK	in	G2	--	3.3V	B2B connector J2-157 / JTAG
TDI	in	F5	--	3.3V	B2B connector J2-159 / JTAG
TDO	out	F6	--	3.3V	B2B connector J2-158 / JTAG
TMS	in	G1	--	3.3V	B2B connector J2-160 / JTAG
VADJ_EN	out	C12	--	3.3V	Power enable signal VADJ
VADJ_VS0	out	F12	--	3.3V	Voltage selection signal VADJ
VADJ_VS1	out	E13	--	3.3V	Voltage selection signal VADJ

Functional Description

JTAG

JTAG access to TEI0006 SoM is only through B2B connector J2 available. The JTAG signals are routed directly from B2B connector through Intel MAX 10 to Intel Cyclone 10 GX.

Access between Intel MAX 10 and Intel Cyclone 10 GX can be selected via the JTAGEN pin. The JTAGEN pin is already pulled up to 3.3V for access to Intel MAX 10. For access to Intel Cyclone 10 GX the JTAGEN pin has to pulled down to GND on B2B connector J2-105.

With carrier board TEIB0006:

DIP-Switch S1-1	JTAG selection
OFF	Intel MAX 10
ON	Intel Cyclone 10 GX

UART

UART signals are routed directly from B2B connector through Intel MAX 10 to Intel Cyclone 10 GX.

B2B		MAX 10		Cyclone 10 GX
J2-153		MAX_IO18		M10_IO1
J2-151		MAX_IO17		M10_IO2

LED and user buttons

The LED1 (B2B connector J2-146) on the TEIB0006 is connected to the user button USER_BTN1 (B2B connector J2-152) and NCONFIG pin. For the other LEDs and user buttons of the TEIB0006 see the table below:

TEIB0006	B2B	MAX10		Cyclone 10 GX	
Signal	Pin location	Signal		Signal	Pin location
USER_BTN1	J2-152	MAX_IO7		NCONFIG	--
USER_BTN2	J2-154	MAX_IO8		INIT_DONE	AA13
LED2	J2-148	MAX_IO6		DEV_CLRN	AC12

The LED 'LED_FP_1' is used as status led:

Blink sequence	Condition	Description
*ooooooo	NCONFIG=0	Cyclone 10 GX is in reset state
**oooooo	NSTATUS=0	Cyclone 10 GX: Error during configuration
***ooooo	--	Power sequencer error
****oooo	--	PLL configuration error
ON	CONF_DONE=0	Cyclone 10 GX is not configured

The following LEDs on the TEI0006 module can be controlled directly by the Cyclone 10 GX:

Cyclone 10 GX			MAX10
Signal	**Pin location**		**LED**
M10_IO3	AC13		LED_FP_2
M10_IO4	AB13		LED_FP_3
DATA0	AE10		LED_FP_4

The signals for the Ethernet LEDs are routed through the MAX10 as follows:

PHY1_LED1 B2B connector J2-67 / PHY1_33LED1

PHY1_LED2 B2B connector J2-69 / PHY1_33LED2

Power

All power regulators are controlled by the power sequencer core. It enables and discharges the power regulators and monitors the power good signals.

The power-up sequence corresponds to Intel's recommendations and is shown in the table below:

Power Group	Power enable	Power good	Notes
0	EN_0V9	PG_0V9	--
1	EN_0V95	PG_0V95	--
2	EN_1V8	PG_1V8	--
3	EN_1V8VIO	PG_1V8VIO	--
	EN_1V35	PG_1V35	--
	EN_VTT	--	--
	VADJ_EN	PG_VADJ	1.8V (default)
	MAX_IO19	MAX_IO20	B2B J2-74/J2-76 / Signals for 3.3V on carrier board TEIB0006 EN_3V3MB /PG_MB_3.3V
	MAX_IO23	MAX_IO22	B2B J2-86/J2-82 / Signals for 1.8V on carrier board TEIB0006 EN_1V8MB /PG_MB_1.8V (required for VCCIO voltage at Bank 2J/2K)

The voltages for Bank 2K (VCCIO2K) and Bank 2J (VCCIO2J) are supplied externally via the B2B connectors (J1-53 /53 and J2-29/30).

Output voltage VADJ of power regulator U11 is set to 1.8V via VADJ_VS0 and VADJ_VS1 pin. Possible selectable voltages are 1.8V, 2.5V and 3.0V.

Reset

The PLL_RST for the programmable Oscillator SI5345A is set to logical one.

Configuration mode selection

The Configuration mode is set to AS/Fast with the MSEL0 and MSEL1 pins.

Programmable Oscillator SI5345A

The volatile memory of the programmable Oscillator SI5345A is configured via I2C interface with following clock frequencies:

PLL out	Mode	Frequency	I/O Standard
OUT0	enabled	100 MHz	LVDS
OUT1	enabled	100 MHz	LVDS
OUT2	enabled	100 MHz	LVCMOS
OUT3	unused	--	--
OUT4	unused	--	--
OUT5	enabled	200 MHz	LVDS
OUT6	enabled	100 MHz	LVDS
OUT7	enabled	125 MHz	LVDS
OUT8	unused	--	--
OUT9	unused	--	--

Appx. A: Change History and Legal Notices

Revision Changes

- REV03 to REV04
  - add status LED
  - rework LED connection to Cyclone 10 GX
  - add external power good signals to power sequencer
  - change configuration mode from AS/Standard to AS/Fast
  - remove SI5345A outputs OUT8 and OUT9
- REV02 to REV03
  - add Power Sequencer Core
  - programm Oscillator SI5345A via I2C interface
- REV01 to REV02
  - add VADJ configuration for power regulator U11

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
		REV04	REV04		• Firmware REV04 release

Error	**Error**		**Error**
r	**r**		**r**
re	**re**		**re**
n	**n**		**n**
d	**d**		**d**
er	**er**		**er**
in	**in**		**in**
g	**g**		**g**
m	**m**		**m**
ac	**ac**		**ac**
ro	**ro**		**ro**
'p	**'p**		**'p**
a	**a**		**a**
g	**g**		**g**
e-	**e-**		**e-**
in	**in**		**in**
fo'	**fo'**		**fo'**
A	A		A
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gu	gu		gu
ou	ou		ou
s	s		s
m	m		m
et	et		et
ho	ho		ho
d	d		d
ov	ov		ov
erl	erl		erl
oa	oa		oa
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2020-01-28	v.3	REV03	REV02	Thomas Dück	• add power sequencer • programming Oscillator SI5345A

2019-08-27	v.1	REV01	REV01	Thomas Dück	• Initial release
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Error rendering macro 'page-info'

Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]