TEB0724 TRM

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Overview

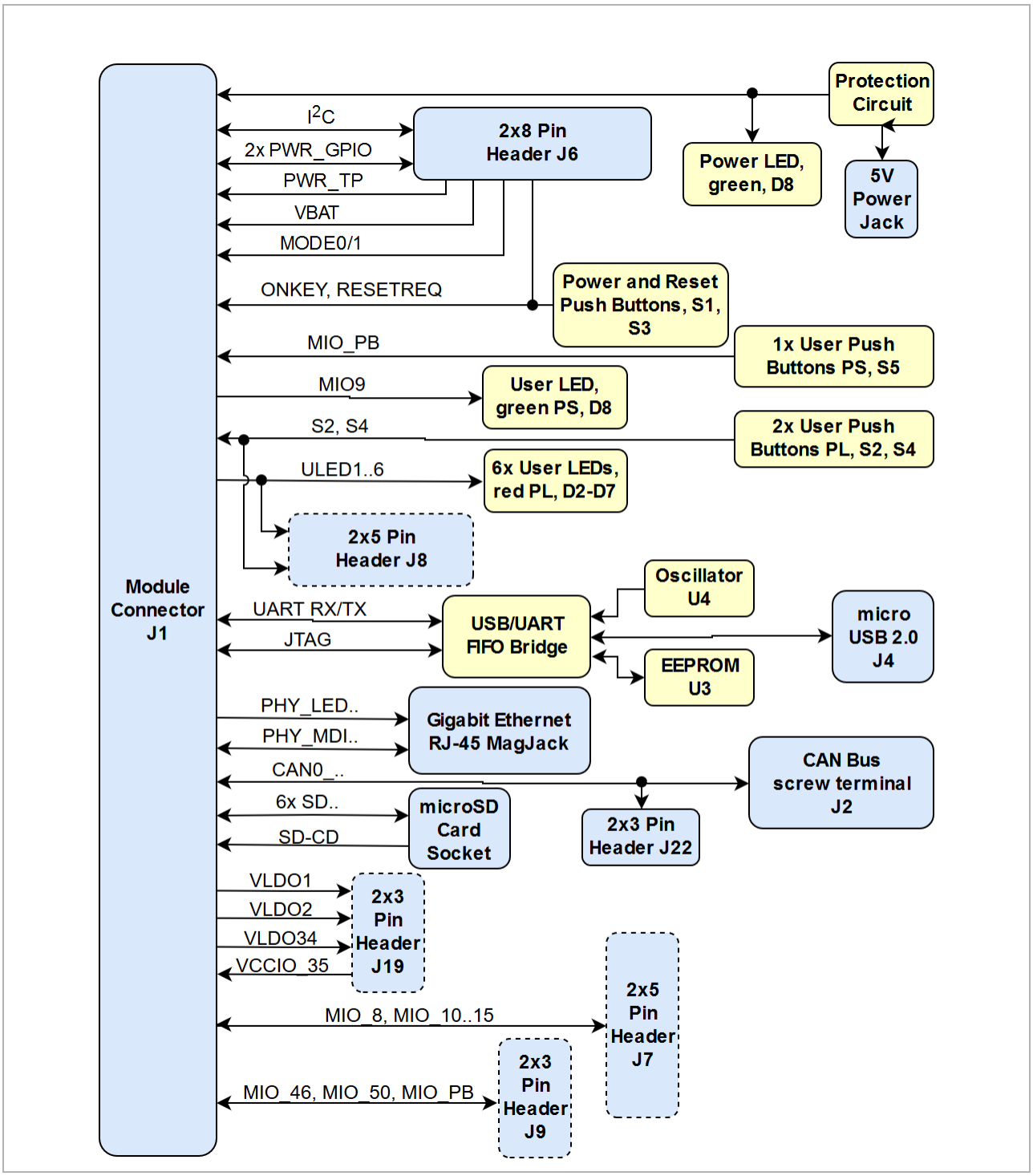
The Trenz Electronic TEB0724-02 is a developement carrier board for the TE0724 and compatible modules. It facilitates easy access to all on the module available features.

Refer to http://trenz.org/teb0724-info for the current online version of this manual and other available documentation.

Key Features

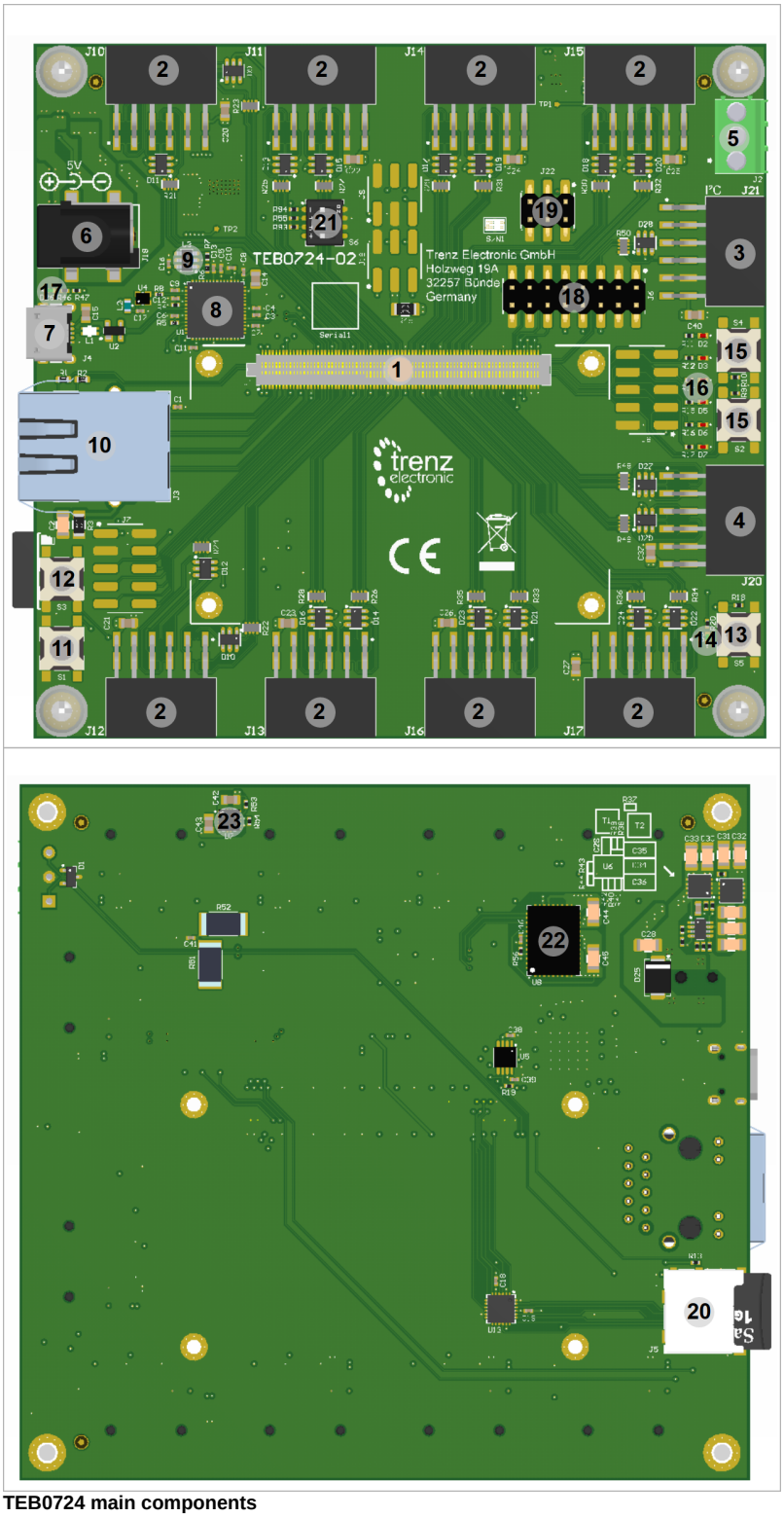
- Samtec 160 pin board to board connector for 4,0 cm x 6,0 cm module
- 10x 2x6 Pin Pmods, (8 usable as dual Pmods, 1x single Pmod, 1x I^2C compatible Pmod)
- MicroUSB to JTAG/UART bridge
- CAN screw terminal
- RJ45 Gigabit Ethernet MagJack connector
- 6x LED, 2x Push Buttons on FPGA
- 1 LED and 1 Push Button on PS
- Power and Reset Push Buttons
- On-board Power Protection Circuit and Power on LED

Block Diagram



TEB0724 block diagram

Main Components



TEB0724 main components

1. Module connector for 4,0x6.0 cm module
2. Pmods usabel as dual Pmods, J10, J11, J12, J13, J14, J15, J16, J17
3. Pmod (single), J20
4. I2C Pmod, J21
5. CAN screw terminal, J2
6. 5V 2.1mm input jack, J18
7. microUSB J4
8. USB to JTAG/UART bridge FT2232H, U1
9. Configuration EEPROM U3
10. RJ45 Gigabit Ehternet Jack, J3
11. Power Button, S1
12. Reset Button, S3
13. User Button PS, S5
14. User LED (green) PS, D8
15. 2x User Button PL, S2, S4
16. 6x User LEDs (red) PL, D2-D7
17. Power LED (green), D36
18. 2x10 Pin header for Boot and Programming options, J6
19. 2x6 Pin header for jumper setting of CAN bus termination resistors, J22
20. microSD Card Slot, J5
21. Dip switches for selecting B_VCCIO_35, S6
22. DCDC (B_VCCIO_35), U8
23. DCDC (B_3.3V), U7

Initial Delivery State

Storage device name	Content	Notes
FTDI Configuration EEPROM U3	Xilinx License	Do not overwrite, see warning in related section

Initial delivery state of programmable devices on the module.

Configuration Signals

The boot device is selected by the mode jumpers on pin header J6. Placing a jumper at pin 13-14 sets Mode0 to low level. Mode1 is set to low level by jumper on pin 15-16. Boot modes are further described at the corresponding section of the modules, e.g. Table 2, Boot mode selection of TE0724 TRM. Default with no jumpers is boot from SD-Card.

Signal	Function	Routed to	B2B Connector Pin	Note
Mode0	bootdevice selection	jumper pins J6-13 J6-14	J1-4	TE0724: pulled up at module
Mode1	bootdevice selection	jumper pins J6-15 J6-16	J1-2	TE0724: pulled up at module
ONKEY	module power signal	push button S1 and pin J6-9	J1-148	TE0724: pulled up at module
RESETREQ	module reset	push button S3 and pin J6-12	J1-150	TE0724: pulled up at module
PWR_GPIO2	-	J6-8	J1-143	User power sequenzing IO
PWR_GPIO4	-	J6-10	J1-141	User power sequenzing IO

Boot process.

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the B2B connector:

B2B Connector	Interfaces	I/O Signal Count	Notes
J1	User IO	72 single ended or 36 differential	9x Pmod
		6 LED	red
		2 Push Button	-
		7 MIO	J7 (not assembled), TE0724: 3.3V
		2 MIO	J9 (not assembled), TE0724: 1.8V
		1 MIO LED	green
		1 MIO Push Button	-
	I²C	2	1x Pmod
	SD IO	7	-
	UART	2	-
	CAN	2	-
	GbE PHY_MDIO + PHY_LEDs	10	-
	JTAG	4	-
	Power GPIO	2	-
	Power/Reset/Fuse programming	3	-
	Bootmode	2	-

General overview of PL I/O signals and SoM's interfaces connected to the B2B connectors

microUSB JTAG/UART Interface

The microUSB connector provides JTAG access to the module through the carriers USB to JTAG/UART bridge, routed to B2B connector J1. The UART is routed via a levelshifter. There is no device with JTAG port on the baseboard.

Signal	B2B Connector Pin
TCK	J1-147
TDI	J1-151
TDO	J1-145
TMS	J1-149
UART RX	J1-36
UART TX	J1-38

JTAG pins connection

SD Card Interface

Connected To	Signal Name	Notes
J1-34	SD-CD	Card detect switch, pulled up, low if card inserted.
J1-24	SD-D0	
J1-22	SD-CMD	
J1-20	SD-CCLK	
J1-26	SD-D1	
J1-28	SD-D2	
J1-30	SD-D3	

SD Card interface signals and connections

Ethernet Interface

The TEB0724 Carrier Board has a RJ45 Gigabit Ethernet MagJack (J3) with two LEDs. On-board Ethernet MagJack pins are routed to B2B connector J1 via MDI. LEDs are also routed to the B2B connector.

Ethernet PHY connection

MagJack	Signal	B2B
J3-2	PHY_MDI0_P	J1-7
J3-3	PHY_MDI0_N	J1-9
J3-4	PHY_MDI1_P	J1-13
J3-5	PHY_MDI1_N	J1-15
J3-6	PHY_MDI2_P	J1-19
J3-7	PHY_MDI2_N	J1-21
J3-8	PHY_MDI3_P	J1-25
J3-9	PHY_MDI3_N	J1-27
J3B	PHY_LED0	J1-10
J3C	PHY_LED1	J1-12

Ethernet Signals

I2C Interface

On-board I^2C bus is accaessable with the following pins:

SDA	SCL	Notes
J1-144	J1-142	B2B

J6-7	J6-5	In-Circuit Programming
J21-10, J21-4	J21-9, J21-3	Pmod

I2C pins

There are no I2C devices on the base board. Pullup resistors have to be provided by the module.

Pmods

The GPIOs of the 10 Pmods (J10 to J17, J20, J21) are connected with 100 Ohm differential routing to the B2B connector. J21 is a pure I^2C compatible Pmod, without additional signals. The other 9 are GPIO Pmods where despite J20 all others can be used as dual Pmods.

Via dip switches S6-1 to S6-3 the variable bank power B_VCCIO_35 for the Pmods J10, J11, J12, J13, J14, J16 can be selected. Respect power regulator limits!

	J10		J11		J12		J13		J14	
PIN	**Signal**	**B2B**	**Signal**	**B2B**	**Signal**	**B2B**	**Signal**	**B2B**	**Signal**	**B2B**
1	PA0_P	J1-56	PB2_N	J1-70	PC2_P	J1-57	PD2_P	J1-77	PE2_N	J1-90
2	PA0_N	J1-58	PB2_P	J1-72	PC2_N	J1-55	PD2_N	J1-75	PE2_P	J1-92
3	PA3_P	J1-46	PB0_N	J1-76	PC0_P	J1-51	PD0_P	J1-71	PE0_N	J1-96
4	PA3_N	J1-48	PB0_P	J1-78	PC0_N	J1-49	PD0_N	J1-69	PE0_P	J1-98
5	GND	-	GND	-	GND	-	GND	-	GND	-
6	VCCIO_35	J1-54	VCCIO_35	J1-54	VCCIO_35	J1-54	VCCIO_35	J1-54	VCCIO_35	J1-54
7	PA1_N	J1-62	PB3_P	J1-68	PC3_N	J1-59	PD3_N	J1-79	PE3_P	J1-88
8	PA1_P	J1-60	PB3_N	J1-66	PC3_P	J1-61	PD3_P	J1-81	PE3_N	J1-86
9	PA2_N	J1-52	PB1_P	J1-82	PC1_N	J1-45	PD1_N	J1-65	PE1_P	J1-102
10	PA2_P	J1-50	PB1_N	J1-80	PC1_P	J1-47	PD1_P	J1-67	PE1_N	J1-100
11	GND	-	GND	-	GND	-	GND	-	GND	-
12	B_VCCIO_35	J1-54	B_VCCIO_35	J1-54	B_VCCIO_35	J1-54	B_VCCIO_35	J1-54	B_VCCIO_35	J1-54

	J15		J16		J17		J20		J21	
PIN	**Signal**	**B2B**	**Signal**	**B2B**	**Signal**	**B2B**	**Signal**	**B2B**	**Signal**	**B2B**
1	PG2_N	J1-110	PF2_P	J1-97	PH2_P	J1-115	PI2_P	J1-133	NC	-
2	PG2_P	J1-112	PF2_N	J1-95	PH2_N	J1-113	PI2_N	J1-131	NC	-
3	PG0_P	J1-114	PF0_P	J1-91	PH0_P	J1-111	PI0_P	J1-129	I2C_SCL	J1-142
4	PG0_N	J1-116	PF0_N	J1-89	PH0_N	J1-109	PI0_N	J1-127	I2C_SDA	J1-144
5	GND	-	GND	-	GND	-	GND	-	GND	-
6	3.3V	J1-74, J1- 43	VCCIO_35	J1-54	3.3V	J1-74, J1- 43	3.3V	J1-74, J1- 43	3.3V	J1-74, J1- 43
7	PG3_P	J1-108	PF3_N	J1-99	PH3_N	J1-117	PI3_N	J1-135	NC	-
8	PG3_N	J1-106	PF3_P	J1-101	PH3_P	J1-119	PI3_P	J1-137	NC	-
9	PG1_N	J1-120	PF1_N	J1-85	PH1_N	J1-105	PI1_N	J1-123	I2C_SCL	J1-142
10	PG1_P	J1-121	PF1_P	J1-87	PH1_P	J1-107	PI1_P	J1-125	I2C_SDA	J1-144
11	GND	-	GND	-	GND	-	GND	-	GND	-
12	3.3V	J1-74, J1- 43	B_VCCIO_35	J1-54	3.3V	J1-74, J1- 43	3.3V	J1-74, J1- 43	3.3V	J1-74, J1- 43

Pmod connections.

CAN Screw Terminal

The CAN bus is routed to screw terminal J2.

PIN	Signal	B2B
J2-1	CAN0_N	J1-1
J2-2	GND	
J2-3	CAN0_P	J1-3

CAN bus connection

Jumpers on J22-1 to J22-3 and J22-2 to J22-4 connect proper split termination resistors to the CAN bus.

Pin Header

Pin Header J6 provides access to power functions, bootmode selection and PMIC In-Circuit Programming (For initial PMIC In-Circuit Programming of the module, Diode D28 has to be removed).

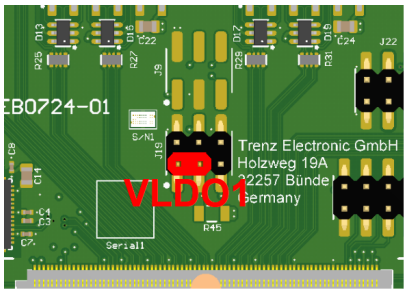
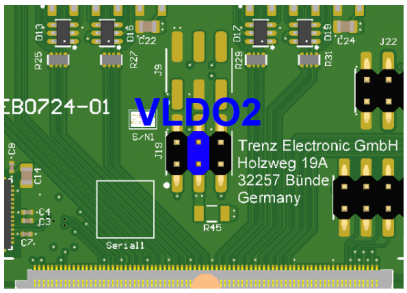
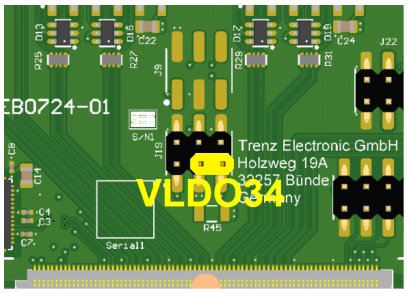
PIN	Signal	B2B
J6-1	VIN	J1-154, J1-156, J1-158, J1-160
J6-2	VIN	J1-154, J1-156, J1-158, J1-160
J6-3	GND	
J6-4	GND	
J6-5	I2C_SCL	J1-142
J6-6	VBAT	J1-152
J6-7	I2C_SDA	J1-144
J6-8	PWR_GPIO2	J1-143
J6-9	ONKEY	J1-148
J6-10	PWR_GPIO4	J1-141
J6-11	PWR_TP	J1-146
J6-12	RESETREQ	J1-150
J6-13	MODE0	J1-2
J6-14	GND	
J6-15	MODE1	J1-4
J6-16	GND	

Pin Header J6

Alternatively to selecting B_VCCIO_35 by using S6 dip switches, VCCIO_35 (e.g. SoM TE0724, Bank 35) can be selected by removing R45 and adding a jumper on optional J19. In table 18 valid jumper positions are given. Voltages and maximum current ratings could be found in the corresponding TRM of the attached module, (e.g. TE0724 TRM#PowerRails).

PIN	Signal	B2B
J19-1	VLDO1	J1-83
J19-2	GND	
J19-3	VCCIO_35	J1-54
J19-4	VLDO2	J1-94
J19-5	VLDO34	J1-53
J19-6	GND	

Optional Pin Header J19

	Jumper position	Signal	e.g. TE0724
	J19 1-3	VLDO1	3.3V
	J19 4-3	VLDO2	1,8V
	J19 5-3	VLDO34	2,5V

J19 Jumper settings for VCCIO_35 voltage selection

Respect VLDO current limitations!

Optional fitted headers J7, J8 and J9 are to provide full access to the Pins at the B2B connector, especially for testing and extension purposes. Description follows below.

PL Button and LED IOs are additionally routed to optionally assembled pin header J8.

PIN	Signal	B2B
J8-1	3.3V	J1-43, J1-74
J8-2	GND	
J8-3	S4	J1-126
J8-4	S2	J1-124
J8-5	ULED5	J1-130
J8-6	ULED6	J1-128
J8-7	ULED3	J1-134
J8-8	ULED4	J1-132
J8-9	ULED1	J1-138
J8-10	ULED2	J1-136

Optional Pin Header J8

Optional pin header J7 gives access to otherwise not used PS MIO IOs at a 3.3V bank.

PIN	Signal	B2B
J7-1	3.3V	43, 74
J7-2	GND	
J7-3	GND	
J7-4	MIO8	J1-14
J7-5	MIO10	J1-31
J7-6	MIO11	J1-33
J7-7	MIO12	J1-35
J7-8	MIO13	J1-37
J7-9	MIO14	J1-39
J7-10	MIO15	J1-41

Optional Pin Header J7

Optional pin header J9 gives access to otherwise not used PS MIO IOs at a 1.8V bank.

PIN	Signal	B2B
J9-1	1.8V	J1-63

J9-2	GND	
J9-3	GND	
J9-4	MIO_46	J1-32
J9-5	MIO_50	J1-40
J9-6	MIO_PB	J1-42

Optional Pin Header J9.

On-board Peripherals

USB to JTAG/UART bridge

The TEB0724 carrier board has on-board microUSB 2.0 (J4) high-speed to UART/FIFO IC FT2232H (U1) from FTDI. Channel A can be used as JTAG Interface (MPSSE) to program on module JTAG devices. Channel B can be used as UART Interface routed via a level shifter to the 1.8V section of the B2B connector, usually connected to the PS of the SoM. There is also a 256-byte serial EEPROM connected to the FT2232H chip pre-programmed with license code to support Xilinx programming tools.

> Do not access the FT2232H EEPROM using FTDI programming tools, doing so will erase normally invisible user EEPROM content and invalidate stored Xilinx JTAG license. Without this license the on-board JTAG will not be accessible any more with any Xilinx tools. Software tools from FTDI website do not warn or ask for confirmation before erasing user EEPROM content.

Oscillators

The module has the following reference clock signals provided by on-board oscillators:

Clock Source	Schematic Name	Frequency	Clock Destination
SiTime SiT8008AI oscillator, U4	OSCI	12.000000 MHz	U1, pin 3.

Reference clock signals

On-board LEDs

LED	Color	Signal	Description and Notes
D1	green	VIN	power indicator
D2-D7	red	ULED1..6	User LED
D8	green	MIO9	MIO user LED
J3B	green	PHY_LED0	Ethernet status
J3C	yellow	PHY_LED1	Ethernet status

On-board LEDs

On-board Push Buttons

Button	Signal	B2B	Description and Notes
S1	ONKEY	J1-148	Power Button, pulled up, on push de-asserted

S3	RESETREQ	J1-150	User LED pulled up, on push de-asserted
S2	S2	J1-124	PL user button, pulled up, on push de-asserted
S4	S4	J1-126	PL user button, pulled up, on push de-asserted
S5	MIO51	J1-42	PS MIO user button, pulled up, on push de-asserted

On-board Push Button

Dip-Switches

Dip-switch S6-1..3 are used to select the adjustable board power. Tabel 14 shows the signals, table 15 how to adjust the switches for corresponding B_VCCIO_35 Voltages.

Switch	Signal
S6-1	VADJ_VS0
S6-2	VADJ_VS1
S6-3	VADJ_VS2
S6-4	NC

Dip-Switches

B_VCCIO_35	S6-1	S6-2	S6-3
3.3V	ON	ON	ON
2.5V	OFF	ON	ON
1.8V	ON	OFF	ON
1.5V	OFF	OFF	ON
1.25V	ON	ON	OFF
1.2V	OFF	ON	OFF

Select B_VCCIO_35 via Dip-Switches.

Power and Power-On Sequence

Power Consumption

Power supply with minimum current capability of 3A for system startup is recommended.

The maximum power consumption depends on the attached module the design running on the module and additional peripherals.

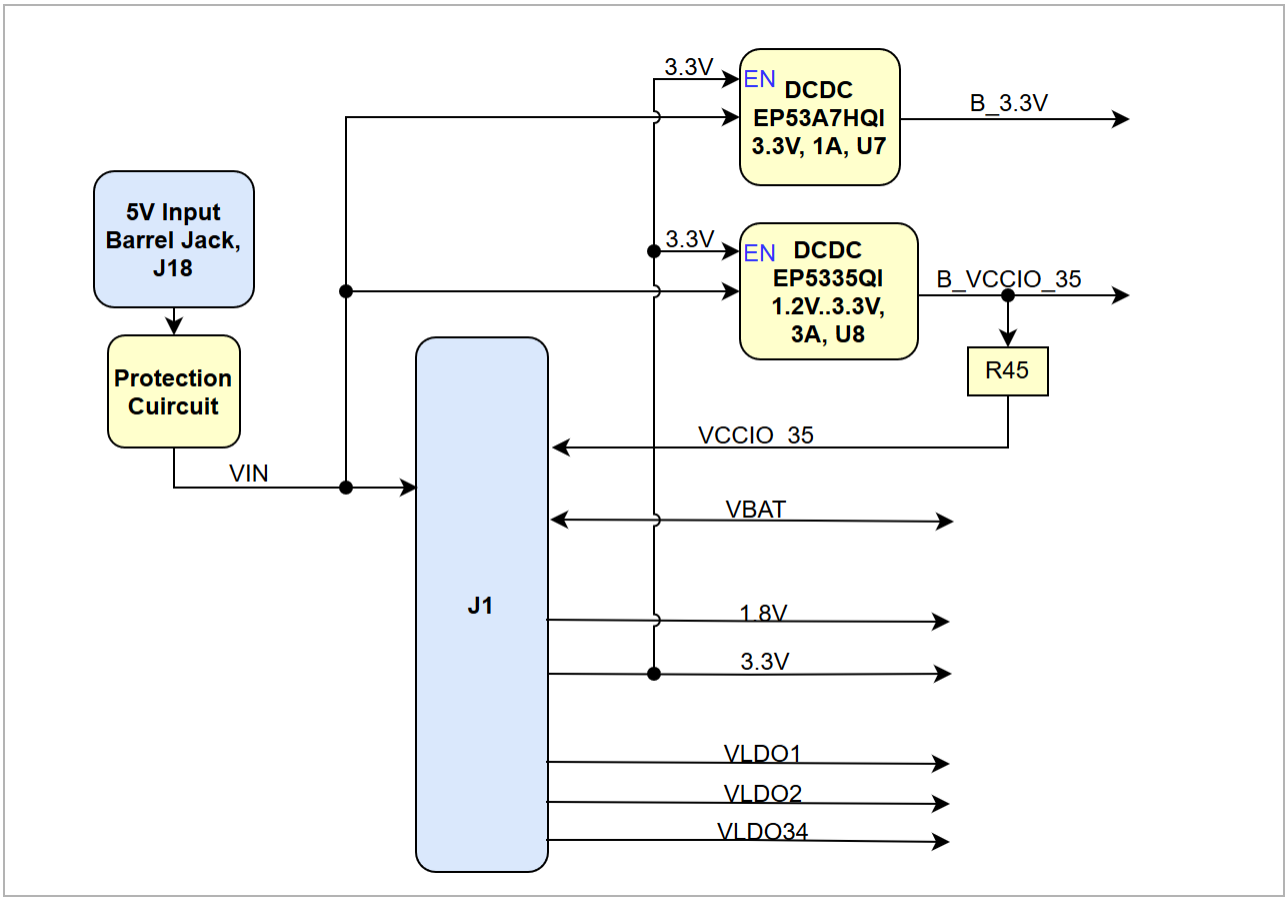
Xilinx provide a power estimator excel sheets to calculate power consumption for FPGAs. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
VIN	340 mA

Power Consumption

To avoid any damage to the base board and attached module, check for stabilized voltages should be carried out (i.e. power good and enable signals) before powering up any SoC's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Power Distribution Dependencies



Power Distribution

User should also check related module documentation and Xilinx data sheet, respectively.

Power-On Sequence

The power-on sequence is solely controlled by the attached module. The baseboard DCDC regulators U7 and U8 are enabled by the 3.3V rail of the module. Optional sequenzing signals for integration of additional hardware are PWR_GPIO2 and PWR_GPIO4.

If the attached module uses an external bank power VCCIO_35, this has to be powered up after the modules SOCs powerrails are up and before any other signal is applied to the bank IOs. The 1.8V and 3.3V power rails are used for the SD Card level shifter U13. The datasheet states to first power up 1.8V and then 3.3V, this has to be taken into account when reconfiguring the power circuit of the attached SoM.

Power-Off is in reverse order. VCCIO_35 has to be disabled before the SoCs core voltages are turned off.

Power Rails

Some of the power rails are sourced by the attached module, see coresponding TRMs of this for further information (e.g. TE0724 TRM#PowerRails).

Power Rail Name	B2B J1 Pins	Direction on B2B	Notes
VIN	154, 156, 158, 160	Output	External main supply voltage (5V).
B_3.3V	-	-	Onboard DCDC.
B_VCCIO_35	-	-	Onboard adjustable DCDC.
3.3V	43, 74	Input	
1.8V	63	Input	
VCCIO_35	54	Output	Connected via 0Ohm R45 to B_VCCIO_35 or source selectable by J19 (R45 removed).
VLDO1	83	Input	(TE0724: 3.3V)
VLDO2	94	Input	Used to enable UART level shifter. Therefore fix at 1.8V.
VLDO34	53	Input	(TE0724: 2.5V)
VBAT	152	Input/Output	Reserved for PMIC backup battery and charger.

Board power rails.

Board to Board Connectors

The module has a 160-pin double-row REF-192552-02 connector on the bottom side. The counterpart REF-192552-01 is placed on the base board.

Order number	REF Number	Samtec Number	Type	Mated Height	Data sheet	Comment
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	5 mm	http://suddendocs.samtec.com/catalog_english/st5.pdf	Standard connector used on module
27219	REF-192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	5 mm	http://suddendocs.samtec.com/catalog_english/ss5.pdf	Standard connector used on board

Connectors.

With different connectors from the used series other mating heights are possible (according to the Datasheet). The module and base board can be manufactured using other connectors upon request.

Connector Specifications	Value
Insulator material	Liquid crystal polymer
Stacking height	5 mm
Contact material	Phosphor-bronze
Plating	Au or Sn over 50 " (1.27 m) Ni
Current rating	1.6 A per pin (2 pins powered)
Operating temperature range	-55 °C to +125 °C
RoHS compliant	Yes

Connector specifications.

Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
5 mm, Single-Ended	13.5GHz / 27Gbps
5 mm, Differential	20GHz / 40Gbps
4 mm, Single-Ended	13GHz / 26Gbps
4 mm, Differential	13.5GHz / 27Gbps

Speed rating.

Current Rating

Current rating of Samtec Razor Beam™ SS5/ST5 B2B connectors is 1.6A per pin (2 pins powered).

Connector Mechanical Ratings

- Shock: 100G, 6 ms sawtooth wave
- Vibration: 7.56G 'RMS', 2 hours per axis, 3 axes total

Manufacturer Documentation

File	Modified
PDF File hsc-report-sma_st5-ss5-04mm_web.pdf	21 09, 2018 by Martin Rohrmüller
PDF File hsc-report-sma_st5-ss5-05mm_web.pdf	21 09, 2018 by Martin Rohrmüller
PDF File ss5_catalog.pdf	21 09, 2018 by Martin Rohrmüller
PDF File ss5-st5_specs.pdf	21 09, 2018 by Martin Rohrmüller

Download All

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	5.5	V	Depends mostly on attached SoM, values here are for TE0724 PMIC, da9062_3v4.pdf.
Storage temperature	-30	80	°C	Push buttons datasheet.

Board absolute maximum ratings.

⚠ Assembly variants for higher storage temperature range are available on request.

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	4.5	5.5	V	Depends mostly on attached SoM, values here are for TE0724 CAN Transceiver, MCP2542FD.
Operating temperature	-25	70	°C	Push buttons datasheet.

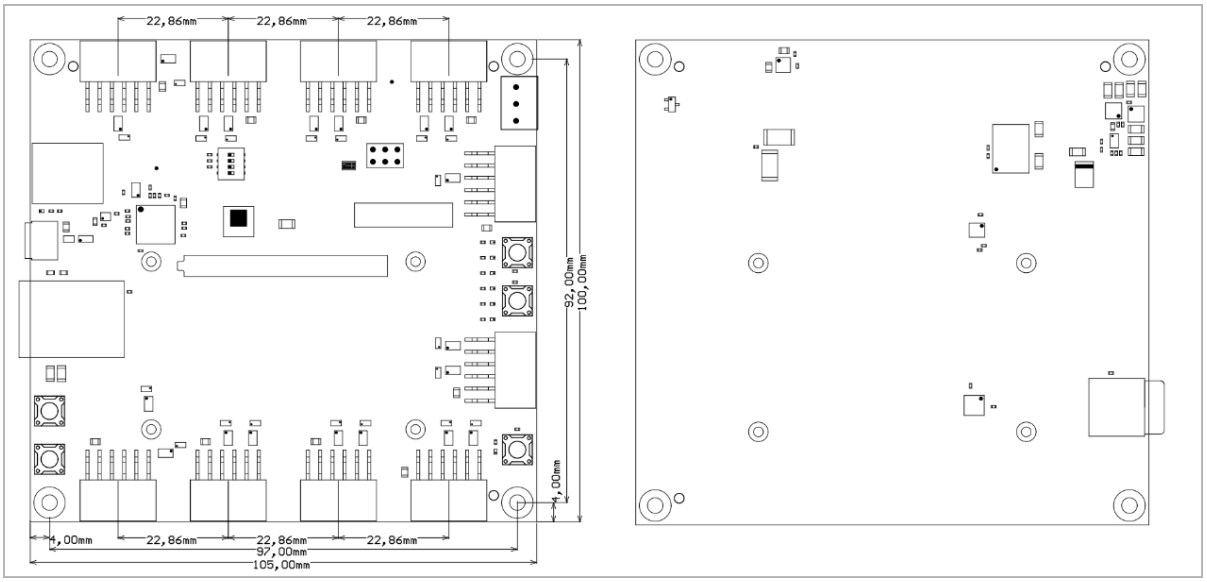
Recommended Operating Conditions.

> ⚠ Please check also the attached SOMs datasheet for a complete list of absolute maximum and recommended operating ratings.

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Physical Dimensions

- Module size: 105 mm × 100 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 4 mm.
- PCB thickness: 1.6 mm.
- Highest part on PCB: approx. 13.5 mm. Please download the step model for exact numbers.



Physical Dimension

Currently Offered Variants

Trenz shop TEB0724 overview page	
English page	German page

Trenz Electronic Shop Overview

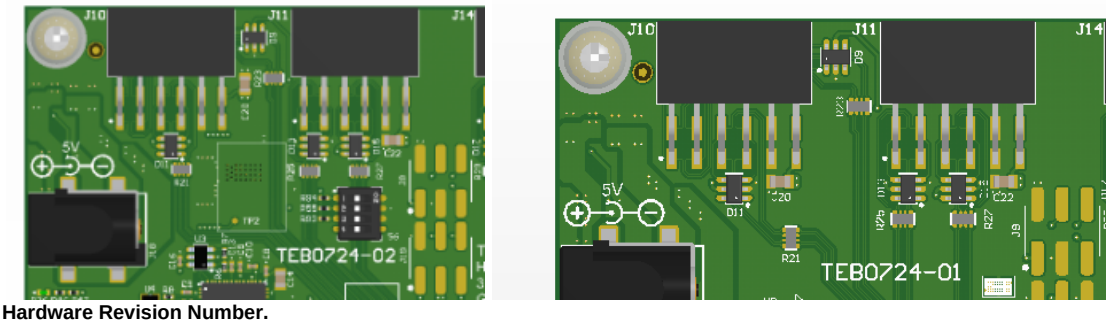
Revision History

Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2018-12-01	02	First production revision		REV02
-	01	Prototypes		REV01

Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.



Hardware Revision Number.

Document Change History

Date	Revision	Contributors	Description

Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• Update Recommended Operating Conditions
03 Apr 2019	v.50	Martin Rohrmüller	• Update to TRM 2.4 style • Corrected Table 15 • Added Comment on Module PMIC in Circuit Programming
23 Nov 2018	v.31	Martin Rohrmüller	• Splitted table 9 in two parts

21 Nov 2018	v.30	Martin Rohrmüller	Update to REV02 • Two DCDCs added, changes in the entire document
02 Oct 2018	v.29	Martin Rohrmüller	• Added Figure J19 Jumper settings • updated Table counter
01 Oct 2018	v.28	Martin Rohrmüller	• Updated assembly pictures • Added typical power consumption • Added hints on power rail voltages
26 Sept 2018	v.27	Martin Rohrmüller	• Updated link to TE0724
24 Sept 2018	v.26	Martin Rohrmüller	• Changed VCCIO_35 connection: R45 not placed , J19 placed
21 Sept 2018	v.25	Martin Rohrmüller	• include B2B infos from general page
07 Sept 2018	v.24	Martin Rohrmüller	• corrected links to connector datasheets

07 Aug 2018	v.23	John Hartfiel	• style update
2018-07-10	v.19	Martin Rohrmüller	• Initial document.

Document change history.

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