Board bring-up overview for TEI0022

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Introduction

Bringing-up SoC boards can be board dependent. Therefore, an overview introducing into the basic requirements to bring-up the board TEI0022 could be very helpful. To reach this goal, this guide shows users with basic knowledge of computers, basic ideas of FPGAs, and Software Design Tools, a detailed insight into the required steps to create the necessary files for booting the Hard Processor System (HPS) of an Intel Cyclone V SoC from an SD card.

The whole design process needs several tools, whereby output files and folders from one step are essential for the next processing step. Therefore, each step can be handled independently with its complexity if the needed files and folders are available. The usage of tools will be described in sequential order, according to the necessary path, booting the HPS. This process is described by showing the requirements in the next section. The following section displays the necessary steps withing the tool "Intel Quartus Prime Project". After that, the generation of the preloader and the main bootloader from u-boot sources is shown, followed by the generation of the device tree blob. Then, the generation of the kernel and the root filesystem is presented which are needed for the SD card setup for the Intel Cycone V HPS which is delivered afterwards. After that, information regarding the boot process, and additional information are given. Finally, references for further information are mentioned.

Requirements

The requirements for bringing up the HPS in the Intel Cyclone V SoC on the TEI0022 consists of the important settings and tools:

- Correct programmed system controller Intel MAX 10 on board TEI0022
- Windows:
  - Intel® Quartus® Prime Lite - Version 18.1 build 625
  - Intel® Soc FPGA Embedded Development Suite (Soc EDS) - Version 18.1 build 625
- Linux:
  - git
  - fdisk
  - make
  - mkfs

Intel Quartus Prime project generation

The first step within the HPS booting procedure is using the tool "Intel Quartus Prime". Within this tool it is necessary to create a new project. After that, it is mandatory to configure the resources (system memory and SD card access) withing the Plattform Designer. After that, connect the basis interfaces (UART, I2C) of the HPS to the board resources and compile the project to create the ".sopinfo", the ".qip" files, and the "handoff" folder. Refer to "Intel Quartus Prime project generation" for more detailed information.

Preloader/Bootloader generation

After Intel Quartus Prime project generation, it is necessary to handle System on Chip (SoC) booting. The boot process, according to the next figure, consists of several stages:

- BootROM:

The BootROM is hard coded into the chip. After reset the BootROM code can detect the selected boot source and perform a minimal HPS setup. After that, the preloader can be loaded into the On Chip RAM (OCRM) and can be executed.

- Preloader:

  While executing the preloader, a further HPS and SDRAM initialization can be done. After that, the bootloader can be loaded and executed. Bootloader and bare metal applications are supported.

- Bootloader:

  The bootloader loads the linux operating system (OS) or a bare metal application into the RAM and starts them. If a linux OS is loaded, the kernel is loaded which loads the linux root file system.

To generate the preloader and the bootloader, the handoff folder, generated in the first stage is used. Refer to "Preloader/Bootloader generation" for more detailed information.

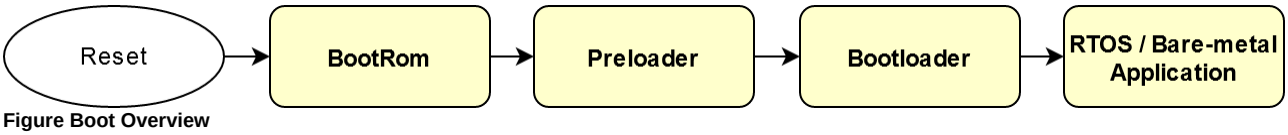

Figure Boot Overview

Device Tree Blob generation

In the third stage, the device tree blob is generated with the ".sopfile" file as input from the Plattform Designer in stage one. Refer to "Device Tree Blob Generation" for more detailed information.

Kernel/Root-filesystem generation

In the fourth stage, the generation of the kernel and the root filesystem with a linux system should be shown. Refer to "Kernel/Root-filesystem generation" for more detailed information.

SD card setup

In the fifth stage, the SD card setup is created to prepare the boot medium to bring-up the HPS within Intel Cyclone V HPS. Refer to "SD card setup" for more detailed information.

Boot Process

In this step, further information regarding the boot process are delivered. Refer to "Boot Process" for more detailed information.

Additional Information

In this section, additional descriptive and explanatory information are given. Refer to "Additional Information" for more detailed information.

References

In this reference section, further additionally information are delivered for deeper investigation.

- Building Bootloader
- Embedded Linux Beginners Guide
- Embedded Peripherals IP User Guide
- Device Tree Generation

- Generating and Compiling the Preloader
- HPS SoC Boot Guide - Cyclone V SoC Development Kit
- Intel® SoC EDS Support
- Intel® SoC FPGA Embedded Development Suite User Guide
- Introducing the Intel® Quartus® Prime Pro and Standard Edition Software User Guides
- Preloader and U-Boot Customization - v13.1
- U-Boot programming: A tutorial -- Part I
- U-Boot programming: A tutorial -- Part II
- U-Boot programming: A tutorial -- Part III

Videos for SoC HPS System Generation

- Preloader and U-boot Generation for Altery Cyclone V SoC
- SoC HPS Quartus II Integration (HW/SW Hand-off)
- SoC HPS System Generation Using Qsys