

TEI0022 Intel MAX 10

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Overview

Firmware for TEI0022 Intel MAX 10 with designator U41: 10M08SAU169C8G

Feature Summary

- Fan control
- JTAG control
- LED control
- UART
- User button
- Power management
 - Power regulator mode control
 - FMC Power control
- Reset management
- Configuration scheme control

Firmware Revision and supported PCB Revision

See Document Change History

Product Specification

Port Description

| Name / opt. VHD Name | Direction | Pin | Bank Power | Description |
|----------------------|-----------|-----|--------------|---|
| BOOTSEL2 | out | L10 | +3.3V | HPS boot select pin 2 |
| CONF_DONE_I | in | L5 | +3.3V | Cyclone V CONF_DONE pin |
| CPU_GPIO_0 | in | N10 | +3.3V | Voltage selection via software for FMC_VADJ (U43 VS0 pin) |
| CPU_GPIO_1 | in | N9 | +3.3V | Voltage selection via software for FMC_VADJ (U43 VS1 pin) |
| CPU_GPIO_2 | in | N11 | +3.3V | Voltage selection via software for FMC_VADJ (U43 VS2 pin) |
| CPU_GPIO_3 | in | L1 | +3.3V | FMC power enable control via software |
| CPU_GPIO_4 | in | H4 | +3.3V | Fan control via software |
| BDBUS0 | in | D1 | +3.3V_MAX10 | FTDI UART TXD pin |
| BDBUS1 | out | C1 | +3.3V_MAX10 | FTDI UART RXD pin |
| EN_0V9 | out | F1 | +3.3V_MAX10 | +0.9V power enable |
| EN_1V8 | out | D12 | +3.3V_MAX10 | +1.8V power enable |
| EN_2V5 | out | A12 | +3.3V_MAX10 | +2.5V power enable |
| EN_3V3 | out | B13 | +3.3V_MAX10 | +3.3V power enable |
| EN_5V0 | out | A7 | +3.3V_MAX10 | +5.0V power enable |
| EN_DDR_FPGA | out | E13 | +3.3V_MAX10 | FPGA DDR power enable |
| EN_DDR_HPS | out | F13 | +3.3V_MAX10 | HPS DDR power enable |
| EN_FMC | out | E1 | +3.3V_MAX10 | FMC_VADJ power enable |
| EN_FMC_3V3 | out | C13 | +3.3V_MAX10 | +3.3V FMC power enable |
| EN_FMC_12V | out | C12 | +3.3V_MAX10 | +12.0V FMC power enable |
| EN_VCC | out | A10 | +3.3V_MAX10 | VCC power enable |
| FAN_EN | out | D13 | +3.3V_MAX10 | Fan control |
| FMC_PG_C2M | out | K7 | +3.3V | FMC power good signal to FMC connector |
| FMC_PRSNT_M2Cn | in | J7 | +3.3V | FMC card detection from FMC connector / currently_not_used |
| FPGA_GPIO_0 | out | K11 | VDD_DDR_FPGA | FPGA IO (FPGA pin AG10) / FPGA UART RXD |
| FPGA_GPIO_1 | in | J10 | VDD_DDR_FPGA | FPGA IO (FPGA pin AH9) / FPGA UART TXD |
| FPGA_RSTn | out | L13 | VDD_DDR_FPGA | FPGA reset |
| FPGA_RSTn_SW | in | B4 | +3.3V_MAX10 | FPGA reset button |
| FMC_TCK | out | M8 | +3.3V | FMC JTAG TCK |
| FMC_TDI | out | M9 | +3.3V | FMC JTAG TDI |
| FMC_TDO | in | M10 | +3.3V | FMC JTAG TDO |
| FMC_TMS | out | M11 | +3.3V | FMC JTAG TMS |
| FPGA_TCK | out | K2 | +3.3V | HPS JTAG TCK |
| FPGA_TDI | out | J1 | +3.3V | FPGA JTAG TDI |
| FPGA_TDO | in | L2 | +3.3V | FPGA JTAG TDO |
| FPGA_TMS | out | J2 | +3.3V | FPGA JTAG TMS |
| FTDI_JTAG_TCK | in | G2 | +3.3V_MAX10 | FTDI JTAG TCK |

| | | | | |
|------------------|-----|-----|-------------|---|
| FTDI_JTAG_TDI | in | F5 | +3.3V_MAX10 | FTDI JTAG TDI |
| FTDI_JTAG_TDO | out | F6 | +3.3V_MAX10 | FTDI JTAG TDO |
| FTDI_JTAG_TMS | in | G1 | +3.3V_MAX10 | FTDI JTAG TMS |
| HPS_TCK | out | K1 | +3.3V | HPS JTAG TCK |
| HPS_TDI | out | M4 | +3.3V | HPS JTAG TDI |
| HPS_TDO | in | J6 | +3.3V | HPS JTAG TDO |
| HPS_TMS | out | M7 | +3.3V | HPS JTAG TMS |
| HPS_RSTn | out | L11 | +3.3V | HPS reset |
| HPS_RSTn_BO | in | K6 | +3.3V | Brown Out detection |
| HPS_RSTn_SW | in | J5 | +3.3V | Reset button |
| HPS_WARM_RSTn | out | M3 | +3.3V | HPS warm reset |
| HPS_WARM_RSTn_SW | in | K5 | +3.3V | HPS warm reset button |
| JTAGSEL0 | in | F9 | +3.3V_MAX10 | Select JTAG connection |
| JTAGSEL1 | in | E9 | +3.3V_MAX10 | Select JTAG connection |
| LED_1V8 | out | H2 | +3.3V_MAX10 | +1.8V power good led |
| LED_FMC_VADJ | out | C9 | +3.3V_MAX10 | FMC_VADJ power good led |
| LED_VCC | out | F12 | +3.3V_MAX10 | VCC power good led |
| LED_VDD_DDR_FPGA | out | E6 | +3.3V_MAX10 | FPGA DDR VDD power good led |
| LED_VDD_DDR_HPS | out | H3 | +3.3V_MAX10 | HPS DDR VDD power good led |
| LED_VTT_DDR_FPGA | out | D6 | +3.3V_MAX10 | FPGA DDR VTT power good led |
| LED_VTT_DDR_HPS | out | G4 | +3.3V_MAX10 | HPS DDR VTT power good led |
| MODE | out | A11 | +3.3V_MAX10 | +5.0V voltage regulator mode selection |
| MODE_DDR_FPGA | out | E10 | +3.3V_MAX10 | Voltage regulator mode selection for FPGA DDR power |
| MODE_DDR_HPS | out | F10 | +3.3V_MAX10 | Voltage regulator mode selection for HPS DDR power |
| MODE_VCC | out | D9 | +3.3V_MAX10 | VCC voltage regulator mode selection |
| MSEL0 | out | N5 | +3.3V | Configuration mode selection pin 0 |
| MSEL1 | out | N3 | +3.3V | Configuration mode selection pin 1 |
| MSEL2 | out | N2 | +3.3V | Configuration mode selection pin 2 |
| MSEL3 | out | N4 | +3.3V | Configuration mode selection pin 3 |
| MSEL4 | out | N6 | +3.3V | Configuration mode selection pin 4 |
| nSTATUS_I | in | L4 | +3.3V | Cyclone V nSTATUS pin |
| PG_1V8 | in | D11 | +3.3V_MAX10 | +1.8V power good signal |
| PG_2V5 | in | C11 | +3.3V_MAX10 | +2.5V power good signal |
| PG_3V3 | in | B12 | +3.3V_MAX10 | +3.3V power good signal |
| PG_5V0 | in | A8 | +3.3V_MAX10 | +5.0V power good signal |
| PG_VCC | in | B11 | +3.3V_MAX10 | VCC power good signal |
| PG_VDD_FPGA | in | E12 | +3.3V_MAX10 | FPGA VDD DDR power good signal |
| PG_VDD_HPS | in | G10 | +3.3V_MAX10 | HPS VDD DDR power good signal |
| PG_VTT_FPGA | in | B10 | +3.3V_MAX10 | FPGA VTT DDR power good signal |
| PG_VTT_HPS | in | B5 | +3.3V_MAX10 | HPS VTT DDR power good signal |

| | | | | |
|---------------------|-----|-----|--------------|--|
| POK_FMC | in | E3 | +3.3V_MAX10 | FMC_VADJ power good signal |
| PWR_SEL | out | E4 | +3.3V_MAX10 | Power selection pin for FMC_VCCPD voltage at U37 (Cyclone V - Bank 8A VCCPD voltage) |
| PWR_SWT_EN | out | C10 | +3.3V_MAX10 | Power enable pin for FMC_VCCPD voltage at U37 |
| STATUS | out | H1 | +3.3V_MAX10 | status led |
| USER_BTN_FPGA | out | G12 | VDD_DDR_FPGA | FPGA user button pin |
| USER_BTN_HPS | out | M2 | +3.3V | HPS user button pin |
| USER_BTN_SW | in | B3 | +3.3V_MAX10 | user button |
| VID0_SW | in | F8 | +3.3V_MAX10 | Dip switch S8A for FMC_VADJ voltage selection |
| VID1_SW | in | E8 | +3.3V_MAX10 | Dip switch S8B for FMC_VADJ voltage selection |
| VID2_SW | in | D8 | +3.3V_MAX10 | Dip switch S8C for FMC_VADJ voltage selection |
| VID0 | out | B2 | +3.3V_MAX10 | Voltage selection pin 0 (VS0) for FMC_VADJ voltage at U43 |
| VID1 | out | C2 | +3.3V_MAX10 | Voltage selection pin 1 (VS1) for FMC_VADJ voltage at U43 |
| VID2 | out | F4 | +3.3V_MAX10 | Voltage selection pin 2 (VS2) for FMC_VADJ voltage at U43 |
| JTAGEN | in | E5 | +3.3V_MAX10 | enable/disable JTAG access to system controller MAX10 |
| BDBUS2 | - | B1 | +3.3V_MAX10 | / currently_not_used |
| BDBUS3 | - | A2 | +3.3V_MAX10 | / currently_not_used |
| BDBUS4 | - | A3 | +3.3V_MAX10 | / currently_not_used |
| BDBUS5 | - | A4 | +3.3V_MAX10 | / currently_not_used |
| BDBUS6 | - | A5 | +3.3V_MAX10 | / currently_not_used |
| BDBUS7 | - | A6 | +3.3V_MAX10 | / currently_not_used |
| CLK_MAX10 | - | H6 | +3.3V | SI5338A CLK2A pin / currently_not_used |
| CLKSEL0 | - | N8 | +3.3V | Cyclone V clock select pin 0 / currently_not_used |
| CLKSEL1 | - | N7 | +3.3V | Cyclone V clock select pin 1 / currently_not_used |
| DEVCLRn | - | B9 | +3.3V_MAX10 | Device-wide reset for MAX 10 / currently_not_used |
| ETH_RST | - | G5 | +3.3V | Ethernet phy reset / currently_not_used |
| FMC_SCL | - | N12 | +3.3V | FMC I ² C interface / currently_not_used |
| FMC_SDA | - | M13 | +3.3V | FMC I ² C interface / currently_not_used |
| FMC_TRST# | - | M12 | +3.3V | FMC JTAG test reset / currently_not_used |
| FPGA_GPIO_2 | - | K12 | VDD_DDR_FPGA | FPGA IO (FPGA pin AF11) / currently_not_used |
| FPGA_GPIO_3 | - | L12 | VDD_DDR_FPGA | FPGA IO (FPGA pin AG11) / currently_not_used |
| FPGA_GPIO_4 | - | G13 | VDD_DDR_FPGA | FPGA IO (FPGA pin AA13) / currently_not_used |
| FPGA_GPIO_5 | - | H13 | VDD_DDR_FPGA | FPGA IO (FPGA pin AB13) / currently_not_used |
| FPGA_GPIO_6 | - | H8 | VDD_DDR_FPGA | FPGA IO (FPGA pin AK2) / currently_not_used |
| FPGA_GPIO_7 | - | H9 | VDD_DDR_FPGA | FPGA IO (FPGA pin AK3) / currently_not_used |
| FPGA_GPIO_8 | - | J9 | VDD_DDR_FPGA | FPGA IO (FPGA pin AJ4) / currently_not_used |
| FPGA_GPIO_9 | - | K10 | VDD_DDR_FPGA | FPGA IO (FPGA pin AK4) / currently_not_used |
| FPGA_GPIO_10 | - | J13 | VDD_DDR_FPGA | FPGA IO (FPGA pin AE13) / currently_not_used |
| FPGA_GPIO_11 | - | J12 | VDD_DDR_FPGA | FPGA IO (FPGA pin AF13) / currently_not_used |
| FPGA_GPIO_12 | - | H10 | VDD_DDR_FPGA | FPGA IO (FPGA pin AD14) / currently_not_used |
| HPS_SPI_SS/BOOTSEL0 | - | K8 | +3.3V | HPS boot select pin 0 / currently_not_used |

| | | | | |
|------------------|---|----|-------|---|
| HPS_TRST# | - | M5 | +3.3V | HPS JTAG test reset / currently_not_used |
| nCONFIG_I | - | M1 | +3.3V | Cyclone V nCONFIG pin / currently_not_used |
| QSPI_CS/BOOTSEL1 | - | J8 | +3.3V | HPS boot select pin 1 / currently_not_used |
| USB_HUB_RST | - | L3 | +3.3V | USB hub (U33) reset / currently_not_used |
| USB_RST | - | H5 | +3.3V | USB phy (U8) reset / currently_not_used |

Functional Description

Fan control

Can be enabled/disabled through the Intel Cyclone V HPS "CPU_GPIO_4" pin.

JTAG control

The FTDI JTAG is connected to the Intel MAX 10, the Intel Cyclone V HPS and Fabric and to the FMC Connector according to the following table.

| JTAGSEL0 | JTAGSEL1 | JTAGEN | JTAG selection |
|-----------|-----------|-----------|----------------|
| X | X | 1 - (ON) | Intel MAX 10 |
| 0 - (ON) | 0 - (ON) | 0 - (OFF) | Cyclone V HPS |
| 0 - (ON) | 1 - (OFF) | 0 - (OFF) | Cyclone V FPGA |
| 1 - (OFF) | 0 - (ON) | 0 - (OFF) | FMC |

LED Control

| Led | Description |
|------------------|--|
| LED_1V8 | connected to PG_1V8 |
| LED_FMC_VADJ | connected to POK_FMC |
| LED_VCC | connected to PG_VCC |
| LED_VDD_DDR_FPGA | connected to PG_VDD_FPGA |
| LED_VDD_DDR_HPS | connected to PG_VDD_HPS |
| LED_VTT_DDR_FPGA | connected to PG_VTT_FPGA |
| LED_VTT_DDR_HPS | connected to PG_VTT_HPS |
| STATUS | <p>Status LED (D25). Status depends on blink sequence and priority.</p> <ol style="list-style-type: none"> 1. LED OFF : no faults 2. *oooooooo : CONF_DONE_I is low-> Cyclone V SoC not programmed 3. **oooooooo : not used 4. ***ooooo : nSTATUS_I failed 5. ****oooo : pressed FPGA_RSTn_SW button 6. ***** : pressed HPS_RSTn_SW / HPS_WARM_RSTn_SW button 7. **** : brown out detection (U54) - HPS_RSTn_BO is low 8. LED ON : not used |

UART

UART signal are routed directly from FTDI chip through Intel MAX 10 to Cyclone V FPGA.

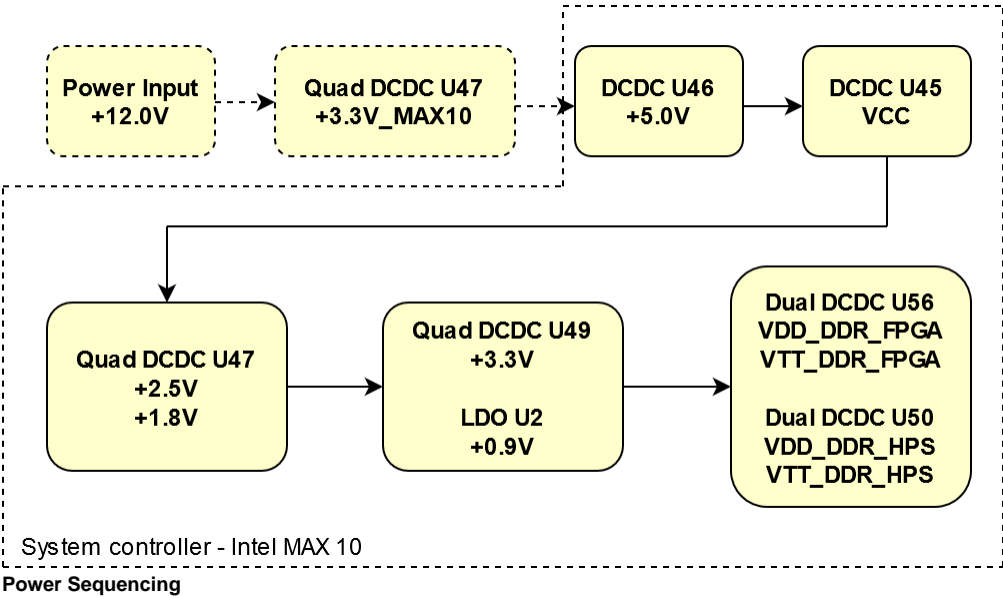
| FTDI FT2232H-56Q | Direction | Cyclone V FPGA |
|------------------|-----------|-----------------------------|
| BDBUS0 (TXD) | | FPGA_GPIO_0 (RXD, Pin AG10) |
| BDBUS1 (RXD) | | FPGA_GPIO_1 (TXD, Pin AH9) |

User button

The user button is connected to the USER_BTN_FPGA pin AB21 and USER_BTN_HPS pin A23 on the Cyclone V FPGA.

Power management

The power sequencing is handled inside the system controller according to the next figure, starting with DCDC U46 +5.0V.



Voltage regulator mode control

| Designator | Signal | State | Description |
|------------|---------------|-------|-----------------------------|
| U45 | MODE_VCC | 1 | Forced continuous mode |
| U46 | MODE | 1 | Forced continuous mode |
| U56 | MODE_DDR_FPGA | 1 | Pulse-skipping mode for VDD |
| U50 | MODE_DDR_HPS | 1 | Pulse-skipping mode for VDD |

For more information about possible modes see datasheet of voltage regulators.

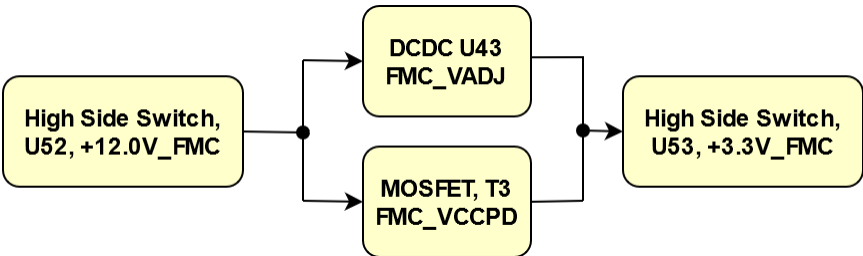
FMC power control

The FMC adjustable voltage selection FMC_VADJ (U43) can be done by the dip switches VID0_SW (S8A), VID1_SW (S8B) and VID2_SW (S8C) or by the Intel Cyclone V HPS via CPU_GPIO_0 pin, CPU_GPIO_1 pin and CPU_GPIO_2 pin. The choice is done according to the next table.

| VID2_SW (S8C)/ CPU_GPIO_2 | VID1_SW (S8B)/ CPU_GPIO_1 | VID0_SW (S8A)/ CPU_GPIO_0 | Voltage | Notes |
|------------------------------|------------------------------|------------------------------|---------------|--|
| ON / 0 | ON / 0 | ON / 0 | 3.3V | - |
| ON / 0 | ON / 0 | OFF / 1 | 2.5V | - |
| ON / 0 | OFF / 1 | ON / 0 | 1.8V | - |
| ON / 0 | OFF / 1 | OFF / 1 | 1.5V | - |
| OFF / 1 | ON / 0 | ON / 0 | 1.25V | - |
| OFF / 1 | ON / 0 | OFF / 1 | 1.2V | - |
| OFF / 1 | OFF / 1 | ON / 0 | 0.8V | not supported by Intel Cyclone V |
| OFF | OFF | OFF | CPU-dependent | select voltages with CPU_GPIO_0/CPU_GPIO_1/CPU_GPIO_2 pins |

The FMC power can be enabled or disabled via software with CPU_GPIO_3 pin, when the dip switches VID0_SW (S8A), VID1_SW (S8B) and VID2_SW (S8C) are set to OFF. If the FMC_VADJ voltage is selected by the dip switches, FMC power is always enabled.

The FMC power sequencing is handled as shown in the next figure.



FMC Power Sequence

Reset Management

The reset buttons are connected via the system controller to the according reset locations.

| Designator | Name | connected to | Notes |
|------------|------------------|---------------|---------------------|
| S1 | HPS_RSTn_SW | HPS_RSTn | Button |
| U54 | HPS_RSTn_BO | HPS_RSTn | Brown out detection |
| S3 | HPS_WARM_RSTn_SW | HPS_WARM_RSTn | Button |
| S4 | FPGA_RSTn_SW | FPGA_RSTn | Button |

Configuration sheme control

| MSEL4 | MSEL3 | MSEL2 | MSEL1 | MSEL0 | Configuration sheme |
|-------|-------|-------|-------|-------|---|
| 0 | 0 | 0 | 1 | 0 | FPP x16 Fast, compression feature enabled |

Appx. A: Change History and Legal Notices

Revision Changes

SC REV03 to REV04

- PCB REV03 support only
- bugfixes
- add status led control
- add USER_BTN_HPS, CONF_DONE_I, nSTATUS_I pins

SC REV02 to REV03

- bugfixes
- add configuration sheme

SC REV01 to REV02

- Changed pin connections
- Changed JTAG connection
- Changed reset connection
- Changed FMC Vadj Voltage selection
- Changed power sequencing

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

| Date | Document Revision | CPLD Firmware Revision | Supported PCB Revision | Authors | Description |
|------|-------------------|------------------------|------------------------|--|---------------------|
| | | REV04 | REV03 | <div>Error rendering macro 'page-info' Ambiguou s method overloadin g for method jdk. proxy279. \$Proxy402 2#hasCon tentLevelP ermission. Cannot</div> | Revision 04 release |

Error rendering macro 'page-info'

Ambiguous method
overloading for method jdk.
proxy279.\$Proxy4022#hasCon
tentLevelPermission. Cannot
resolve which method to
invoke for [null, class java.lang.
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confluence.pages.Page] due
to overlapping prototypes
between: [interface com.
atlassian.confluence.user.
ConfluenceUser, class java.
lang.String, class com.
atlassian.confluence.core.
ContentEntityObject] [interface
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atlassian.confluence.core.
ContentEntityObject]

Error rendering macro 'page-info'

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overloading for method jdk.
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confluence.pages.Page] due
to overlapping prototypes
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atlassian.confluence.user.
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lang.String, class com.
atlassian.confluence.core.
ContentEntityObject] [interface
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| 2020-06-03 | v.9 | REV03 | REV02 | Thomas Dück | Revision 03 release |
| 2020-02-19 | v.7 | REV02 | REV02 | <div> Error rendering macro 'page- info' Ambiguou s method overloadin g for method jdk. proxy279. \$Proxy402 2#hasCon tentLevelP ermission. Cannot resolve which method to invoke for [null, class java. lang. </div> | Initial release |

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| | | | | <div>ContentEntityObject]</div> | |
| | All | | | <div><div>Error rendering macro 'page-info'</div><div>Ambiguous methods overloading for method jdk.proxy279.\$Proxy402#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping</div></div> | |

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Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no [SVHC \(Substances of Very High Concern\) on the Candidate List](#) are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the [European Chemicals Agency \(ECHA\)](#).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

Error rendering macro 'page-info'

Ambiguous method overloading for method `jdk.proxy279.$Proxy4022#hasContentLevelPermission`. Cannot resolve which method to invoke for `[null, class java.lang.String, class com.atlassian.confluence.pages.Page]` due to overlapping prototypes between: `[interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]` `[interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]`