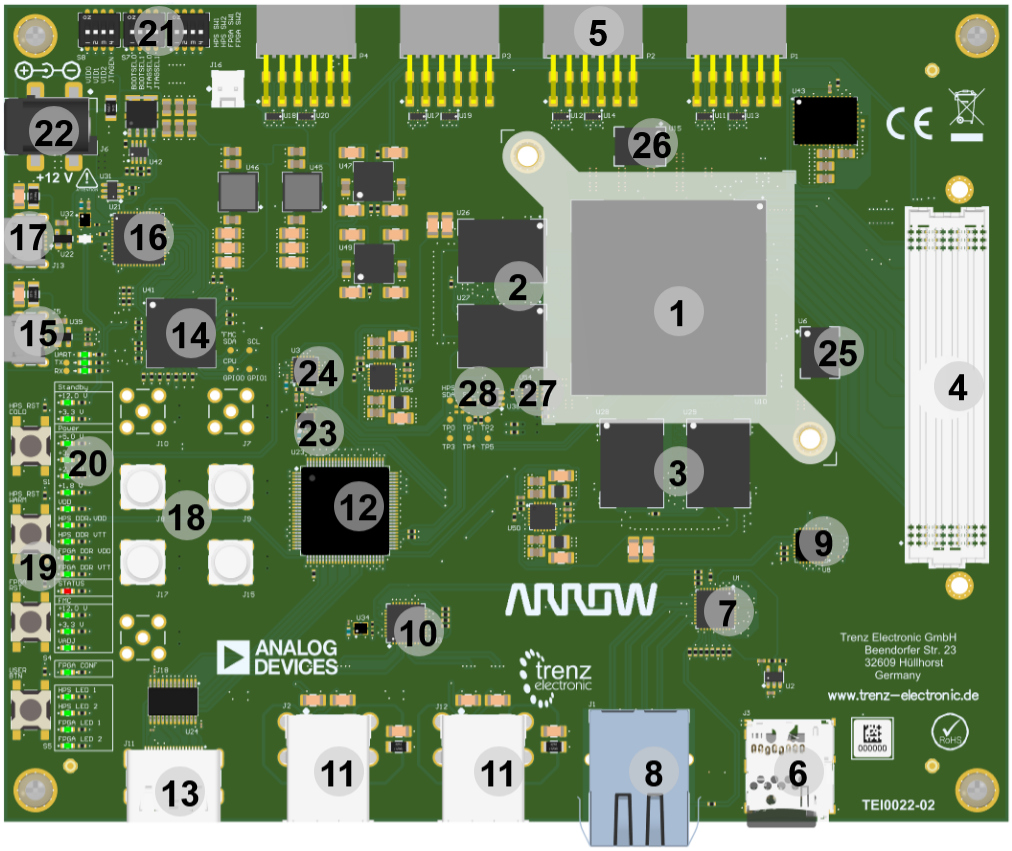
TEI0022 Getting Started

Table of Contents

Overview

Basic instructions to work with TEI0022.

> Functionality of buttons, DIP switches, and LEDs depends on CPLD Firmware.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Trenz Electronic GmbH
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32609 Hüllhorst
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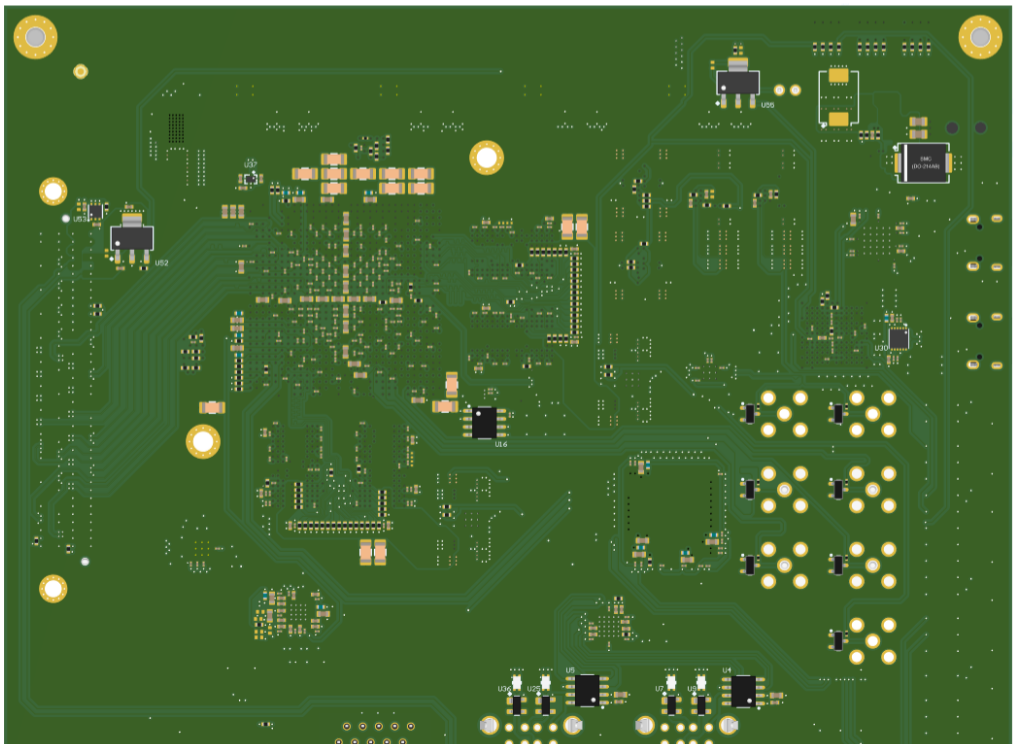
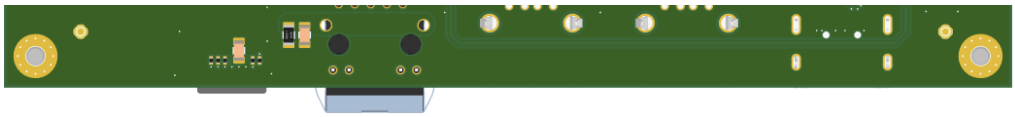
TEI0022-02





Board Overview

Board Overview

Number	Note	Number	Note
1	U10 - Intel Cyclone V	15	J5 - Micro USB for UART
2	U26...27 - DDR3 for Fabric	16	U21 - USB to JTAG FTDI
3	U28...29 - DDR3 for HPS	17	J13 - Micro USB for JTAG
4	J4 - FMC	18	J7...10 / J15 / J17...18 - SMA Connector
5	P1...4 - PMOD	19	S1, S3...5 - Button
6	J3 - SD Card	20	LEDs
7	U1 - Ethernet PHY	21	S2 / S7...8 - DIP Switch
8	J1 - Ethernet RJ45	22	J6 - Power Jack
9	U8 - USB PHY	23	U48 - Oscillator
10	U33 - USB HUB	24	U3 - Programmable Clock Generator
11	J2/ J12 - USB Connector	25	U6 - QSPI
12	U23 - HDMI Transmitter	26	U15 - QSPI
13	J11 - HDMI Connector	27	U54 - Power Monitoring
14	U41 - Intel MAX 10	28	U38 - EEPROM

Power supply

Single +12.0 V power supply is needed to power on the board at power jack J6. Current depends mainly on design and cooling solution. Use Intel Power Estimator and/or your Intel Quartus Prime Project to estimate min current. Minimum of 3A are recommended for basic functionality.

DIP-Switches and Push Buttons

There are three four-bit dip switches and four buttons, explained in the following:

Overview 21	Default	Description	Active Level
S2-1	OFF	HPS User Switch 1	L
S2-2	OFF	HPS User Switch 2	L
S2-3	OFF	FPGA User Switch 1	L
S2-4	OFF	FPGA User Switch 2	L

DIP Switche S2

Overview 21	Default	Description	Active Level
S7-1	OFF		L

S7-1	S7-2	Boot Selection
0	0	FPGA

S7-2	ON	1	0	SD/MMC	L
		1	1	SPI	
S7-3	ON				L
S7-4	OFF				L

S7-3	S7-4	S8-4	JTAG Selection
X	X	ON	MAX 10
ON	ON	OFF	HPS
ON	OFF	OFF	FPGA
OFF	ON	OFF	FMC

DIP Switche S7 (Firmware dependent)

Overview 21	Default	Description	Active Level
S8-1	OFF		L
S8-2	OFF		L
S8-3	OFF		L
S8-4	OFF		H

S8-3	S8-2	S8-1	Output Voltage
ON	ON	ON	3.3 V
ON	ON	OFF	2.5 V
ON	OFF	ON	1.8 V
ON	OFF	OFF	1.5 V
OFF	ON	ON	1.25 V
OFF	ON	OFF	1.2 V
OFF	OFF	ON	0.8 V (not supported by Intel Cyclone V)
OFF	OFF	OFF	Selected by HPS (Firmware dependent)

S7-3	S7-4	S8-4	JTAG Selection
X	X	ON	MAX 10
ON	ON	OFF	HPS
ON	OFF	OFF	FPGA
OFF	ON	OFF	FMC

DIP Switche S8 (Firmware dependent)

Overview 21	Default	Description	Active Level
S1	OFF	Intel Cyclone V HPS Reset	L
S3	OFF	Intel Cyclone V HPS Warm Reset	L
S4	OFF	Intel Cyclone V FPGA Reset	L
S5	OFF	Intel Cyclone V User Button	L

Push Button (Firmware dependent)

LEDs

The LED functionality is explained in the following:

Designator	Color	Connected to	Active Level	Note
J1C	Yellow	Ethernet PHY	L	Ethernet Status
D25	Red	Intel MAX 10	H	Board Status
D11	Green	Intel Cyclone V HPS	H	HPS User LED 2

D12	Green	Intel Cyclone V HPS	H	HOS User LED 1
D13	Green	Intel Cyclone V FPGA	H	FPGA User LED 2
D14	Green	Intel Cyclone V FPGA	H	FPGA User LED 1
D8	Green	Intel MAX 10 and Intel Cyclone V	L	Programming Status
D15	Green	UART FTDI	L	UART Status
D18	Green	UART TX	L	UART TX Status
D19	Green	UART RX	L	UART RX Status
D21	Green	+12.0V	H	+12.0 V Status
D1	Green	+12.0V_FMC	H	+12.0 V FMC Status
D2	Green	+5.0V	H	+5.0 V Status
D3	Green	+3.3V	H	+3.3 V Status
D20	Green	+3.3V_MAX10	H	+3.3 V Standby Status
D22	Green	+3.3V_FMC	H	+3.3 V FMC Status
D4	Green	+2.5V	H	+2.5 V Status
D5	Green	Intel MAX 10	H	+1.8 V Status
D7	Green	Intel MAX 10	H	VCC Status
D9	Green	Intel MAX 10	H	VADJ Status
D6	Green	Intel MAX 10	H	FPGA DDR VDD Status
D23	Green	Intel MAX 10	H	HPS DDR VDD Status
D17	Green	Intel MAX 10	H	HPS DDR VTT Status
D10	Green	Intel MAX 10	H	FPGA DDR VTT Status

LEDs (Firmware dependent)

JTAG/UART

JTAG and UART connections are available through mini USB connectors.

Designator	Connected to	Direction	Note
J13	Intel MAX 10 via FTDI	IN	JTAG
J5	Intel Cyclone V via FTDI	-	UART

JTAG and UART

Reference Designs

- TEI0022 Reference Designs

Notes

- TEI0022 Resources
  - Board bring-up overview for TEI0022 - basic steps to create a design (Important some configuration can be vary for different assembly /PCB version)