TE0823 Test Board

Table of contents

Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW Manager
Wiki Resources page: https://trenz.org/te0823-info

Key Features

- Vitis/Vivado 2022.2
- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- MAC from EEPROM
- User LED
- Modified FSBL for SI5338 programming

Revision History

Date	Vivado	Project Built	Authors	Description
2023-09-20	2022.2	TE0823-test_board-vivado_2022.2-build_8_20230920091958.zip TE0823-test_board_noprebuilt-vivado_2022.2-build_8_20230920091958.zip	Manuela Strücker	• Release Vivado 2022.2 • new variants
2022-11-08	2021.2.1	TE0823-test_board_noprebuilt-vivado_2021.2-build_20_20221108082219.zip TE0823-test_board-vivado_2021.2-build_20_20221108082219.zip	Manuela Strücker	• bugfix uncomment block design modifications in mod_bd.tcl • added jtag2axi for test purposes
2022-10-25	2021.2.1	TE0823-test_board_noprebuilt-vivado_2021.2-build_19_20221025110452.zip TE0823-test_board-vivado_2021.2-build_19_20221025110452.zip	Manuela Strücker	• Release Vivado 2021.2.1 • script update

2021-10-27	2020.2	TE0823-test_board_noprebuilt-vivado_2020.2-build_8_20211027094814.zip TE0823-test_board-vivado_2020.2-build_8_20211027094802.zip	Mohsen Chamanbaz /John Hartfiel	• replace 19.2 fsbl template with 20.2 • new variants
2021-08-24	2020.2	TE0823-test_board_noprebuilt-vivado_2020.2-build_7_20210824103952.zip TE0823-test_board-vivado_2020.2-build_7_20210824103936.zip	Mohsen Chamanbaz	• startup application added • webfwu application added
2021-08-17	2020.2	TE0823-test_board_noprebuilt-vivado_2020.2-build_7_20210817113507.zip TE0823-test_board-vivado_2020.2-build_7_20210817113435.zip	Mohsen Chamanbaz	• 2020.2 release
2020-03-16	2019.2	TE0823-test_board-vivado_2019.2-build_8_20200316163150.zip TE0823-test_board_noprebuilt-vivado_2019.2-build_8_20200316163202.zip	John Hartfiel	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated for Vivado versions below /equal to 2021.2 and 2021.2.1 patch, see Xilinx Forum Request	use corresponding board files for the Vivado versions	--

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2022.2	needed Vivado is included into Vitis installation
PetaLinux	2022.2	needed

SI ClockBuilder Pro	---	optional

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0823-01-3PIU1FL	3cg_1li_1gb	REV01	1GB	128MB	8GB	NA	Low Profile Connector
TE0823-01-3PIU1FA	3cg_1li_1gb	REV01	1GB	128MB	8GB	NA	NA
TE0823-01-S001	3cg_1li_2gb	REV01	2GB	128MB	8GB	NA	Custom, AN: 3PI?1FA
TE0823-01-3PIU1ML	3cg_1li_1gb	REV01	1GB	128MB	8GB	NA	Low Profile Connector, other emmC Manuf.
TE0823-01-3PIU1MA	3cg_1li_1gb	REV01	1GB	128MB	8GB	NA	other emmC Manuf.
TE0823-01-S002	3cg_1li_2gb	REV01	2GB	128MB	8GB	NA	Custom, other emmC Manuf., AN: 3PI?1FA
TE0823-01-3PIU1MAZ	3cg_1li_1gb	REV01	1GB	128MB	8GB	NA	other emmC Manuf.
TE0823-01-S003	3cg_1li_2gb	REV01	2GB	128MB	8GB	NA	Custom, other emmC Manuf., AN: 3PI?1FA

*used as reference

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TE0703*	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers • Used as reference carrier.

TE0705	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TE0706	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers
TEBA0841	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support
TEF1002	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers

*used as reference

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

*used as reference

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
SI5338	<project folder>\misc\PLL\Si5338	SI5338 Project with current PLL Configuration
init.sh	<project folder>\misc\sd	Additional Initialization Script for Linux

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0823 "Test Board" Reference Design

Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- Vivado Projects - TE Reference Design
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths---------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-------------------------------------------------------------------
-------------------------TE Reference
Design---------------------------
-------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

> ⚠ Note: Select correct one, see also Vivado Board Part Flow

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "<project folder>\prebuilt\hardware\<short name>")

```
TE::hw_build_design -export_prebuilt
```

> ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
   - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr
7. Generate Programming Files with Vitis (recommended)
   a. Copy PetaLinux build image files to prebuilt folder
      - copy **u-boot.elf, system.dtb, bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

      > ⓘ "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

   b. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or
start with TE Scripts on Vivado TCL)
```

> ⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis

8. Generate Programming Files with Petalinux (alternative), see PetaLinux KICKstart

Launch

Programming

> Check Module and Carrier TRMs for proper HW configuration before you try any design.
>
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select Create and open delivery binary folder

> Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs BOOT.bin on QSPI flash)
`TE::pr_program_flash -swapp u-boot` `TE::pr_program_flash -swapp hello_te0823 (optional)`

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
    - Depends on Carrier, see carrier TRM.

SD-Boot mode

1. Copy **image.ub**, **boot.src** and **Boot.bin** on **SD**
    - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries
    - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
    - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)

> Note: See TRM of the Carrier, which is used.

> Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
> The boot options described above describe the common boot processes for this hardware; other boot options are possible.
> For more information see Distro Boot with Boot.scr

4. Power On PCB

   1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD/QSPI Flash into OCM

   2. FSBL init PS, programs PL using the bitstream and loads U-boot from SD into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - Select COM Port

   > Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

```
# password disabled
petalinux login: root
Password: root
```

   > Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0        (check I2C 0 Bus)
dmesg | grep rtc        (RTC check)
udhcpc                                (ETH0 check)
lsusb                                (USB check)
```

4. Option Features

- Webserver to get access to Zynq
    - insert IP on web browser to start web interface
- init.sh scripts
    - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

Vivado HW Manager

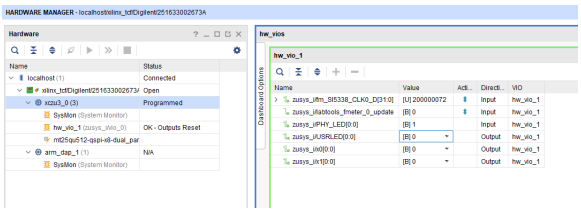
Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

Control:

- GTR Power: set X0=0 and X1=1 to disable GTR Power
- USER LED: On/OFF

Monitoring:

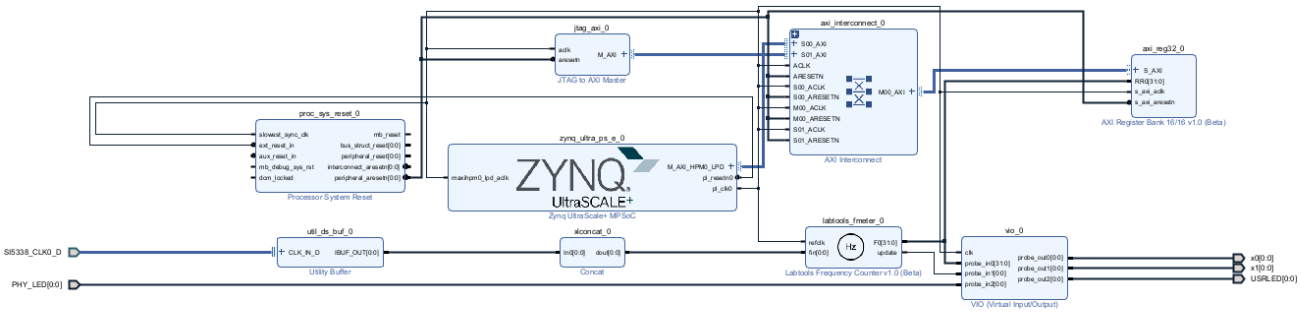
- SI5338_CLK0 Counter: 200MHz with example Design
    - Set radix from VIO signals to unsigned integer.
      Note: Frequency Counter is inaccurate and displayed unit is Hz
- ETH PHY LEDs



Vivado Hardware Manager

System Design - Vivado

Block Design



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO, USB2 only

PS Interfaces

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design
```

Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN B13 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN B14 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]

set_property PACKAGE_PIN C13 [get_ports {PHY_LED[0]}]
set_property PACKAGE_PIN C14 [get_ports {PHY_LED[1]}]
set_property IOSTANDARD LVCMOS18 [get_ports {PHY_LED*}]
set_property PACKAGE_PIN A15 [get_ports {USRLED[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {USRLED*}]
set_property PACKAGE_PIN B14 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis

Application

Template location: "<project folder>\sw_lib\sw_apps\"

zynqmp_fsbl

TE modified 2022.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration
    - ETH+OTG Reset over MIO

zynqmp_pmufw

Xilinx default PMU firmware.

hello_te0823

Hello TE0823 is a Xilinx Hello World example as endless loop instead of one console output.

u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- select SD default instead of eMMC:
  - CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- add new flash partition for bootscr and sizing
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART0_SIZE=0x2000000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART1_SIZE=0x2000000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART2_SIZE=0x40000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_NAME="bootscr"
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_SIZE=0x80000
- Identification
  - CONFIG_SUBSYSTEM_HOSTNAME="trenz"
  - CONFIG_SUBSYSTEM_PRODUCT="TE0823"

U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- MAC from eeprom together with uboot and device tree settings:
  - CONFIG_ENV_OVERWRITE=y
  - CONFIG_ZYNQ_MAC_IN_EEPROM is not set
  - CONFIG_NET_RANDOM_ETHADDR is not set
- Boot Modes:
  - CONFIG_QSPI_BOOT=y
  - CONFIG_SD_BOOT=y
  - CONFIG_ENV_IS_IN_FAT is not set
  - CONFIG_ENV_IS_IN_NAND is not set
  - CONFIG_ENV_IS_IN_SPI_FLASH is not set
  - CONFIG_SYS_REDUNDAND_ENVIRONMENT is not set
  - CONFIG_BOOT_SCRIPT_OFFSET=0x4040000
- Identification
  - CONFIG_IDENT_STRING=" TE0823"

Change platform-top.h:

```
#include <configs/xilinx_zynqmp.h>
#no changes
```

Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"

/*----------------------- SD1 sd2.0 -----------------------*/
&sdhci1 {
    disable-wp;
    no-1-8-v;
};


/*----------------------- USB 2.0 only --------------------*/
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
    snps,dis_u2_susphy_quirk;
    snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};


/*------------------------- ETH PHY -----------------------*/
&gem3 {
    /delete-property/ local-mac-address;
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};


/*------------------------- QSPI ------------------------- */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};
```

```
/*---------------------------- I2C ------------------------*/
&i2c0 {
    eeprom: eeprom@50 {
        compatible = "microchip,24aa025", "atmel,24c02";
        reg = <0x50>;

        #address-cells = <1>;
        #size-cells = <1>;
        eth0_addr: eth-mac-addr@FA {
          reg = <0xFA 0x06>;
        };
    };
};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- Only needed to fix JTAG Debug issue:
    - CONFIG_CPU_FREQ is not set

Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
    - CONFIG_busybox-httpd=y
- For additional test tools only:
    - CONFIG_i2c-tools=y
    - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils, usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- For auto login:
    - CONFIG_auto-login=y
    - CONFIG_ADD_EXTRA_USERS="root:root;petalinux:;"

FSBL patch (alternative for vitis fsbl trenz patch)

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw"

te_* files are identical to files in "<project folder>\sw_lib\sw_apps\zynqmp_fsbl\src" except for the PLL files (SI5338) which depend on PLL revision. The PLL files may have to be copied again manually into the appropriate petalinux folder "<project folder>\os\petalinux\project-spec\meta-user\recipes-bsp\embeddedsw\fsbl-firmware\git\lib\sw_apps\zynqmp_fsbl\src"

Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

startup

Script App to load init.sh from SD Card if available.

webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

Additional Software

SI5338

File location "<project folder>\misc\PLL\Si5338\Si5338-*.slabtimeproj"

General documentation how you work with these project will be available on Si5338

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy241.$Proxy3496#ha	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#ha	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#ha	• Release Vivado 2022.2 • new variants

sContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class

sContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class

sContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class

java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject] [interfac e com. atlassian .user. User, class java. lang. String, class com. atlassian . confluen ce.core. Content EntityOb ject]	
2022-11.18	v.13	Manuela Strücker	• bugfix uncomment block design modifications in mod_bd.tcl • added jtag2axi for test purposes

2022-10-25	v.11	Manuela Strücker	• Release Vivado 2021.2.1 • script update
2022-10-27	v.9	John Hartfiel	• new design files and variants
2021-08-24	v.8	John Hartfiel	• startup application added • webfwu application added
2021-08-18	v.7	Mohsen Chamanbaz	• 2020.2 release
2020-03-17	v.4	John Hartfiel	• 2019.2 release
	All	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy241.$Proxy3496#hasContentLevelPermission. Cannot resolve which	

method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.

		confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	

Document change history.

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Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

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Error rendering macro 'page-info'

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