TE0820 HDMI701

Table of contents

Overview

Refer to http://trenz.org/te0820-info for the current online version of this manual and other available documentation.

Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- Linux Debian 9 (Stretch) or Linux Ubuntu 18.04 (Bionic Beaver)
- HDMI
- SD
- ETH (use EEPROM MAC)
- USB
- I2C
- TE0701
- RTC
- Modified FSBL for SI5338 programming and DMA (for HDMI)
- Special FSBL for QSPI programming

Revision History

Date	Vivado	Project Built	Authors	Description
2020-03-27	2019.2	TE0820-HDMI701_noprebuilt-vivado_2019.2-build_8_20200330084946.zip TE0820-HDMI701-vivado_2019.2-build_8_20200330084931.zip	Mohsen Chamanbaz	• initial release

Design Revision History

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Known Issues

Requirements

Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SD Card Formatter		format SD Card
Win32 DiskImager		born generated image on SD

Software

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~TE0820-ES1~~	~~es1~~	~~REV01~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	Not longer supported by vivado
~~TE0820-02-02EG-1E~~	2eg_1e_1gb	REV02	1GB	64MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-02EG-1E3~~	2eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-02CG-1E~~	2cg_1e_1gb	REV02	1GB	64MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-03EG-1E~~	3eg_1e_1gb	REV02	1GB	64MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-03EG-1E3~~	3eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-03CG-1E~~	3cg_1e_1gb	REV02	1GB	64MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-02EG-1EA~~	2eg_1e_1gb	REV02	1GB	128MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-02EG-1EL~~	2eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-02CG-1EA~~	2cg_1e_1gb	REV02	1GB	128MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-03EG-1EA~~	3eg_1e_1gb	REV02	1GB	128MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-03EG-1EL~~	3eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-03CG-1EA~~	3cg_1e_1gb	REV02	1GB	128MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
~~TE0820-02-04CG-1EA~~	4cg_1e_1gb	REV02	1GB	128MB	4GB	NA	not supported on this demo (changes into FSBL and device tree template are need)
TE0820-03-04EV-1EA	4ev_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02CG-1EA	2cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EA	2eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EL	2eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-03CG-1EA	3cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-04CG-1EA	4cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-2AI21FA	2cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FL	2eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-3AI210A	3cg_1i_2gb	REV03	2GB	128MB	0GB	NA	NA
TE0820-03-3BE21FA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-3BE21FL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-02CG-1ED	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA

TE0820-03-2AE21FA	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FA	2eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AE21FA	3cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AI21FA	3cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4AE21FA	4cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FA	4ev_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DI21FA	4ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA

Hardware Modules

Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers

Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
Cooler	It's recommended to use cooler on ZynqMP device
USB Cable	Connect to USB2 or better USB3 Hub for proper power supply over USB
Monitor	DELL Model Number: U2412Mc
Micro USB to USB A Adapter	Adapter for USB Hub
USB HUB	To connnect Mouse and Keyboard simultaneously
Keyboard	need for Ubuntu/Debian GUI
Mouse	need for Ubuntu/Debian GUI
HDMI Cable	--

Additional Hardware

Content

For general structure and of the reference design, see Project Delivery - AMD devices

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
Vitis	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Design sources

Additional Sources

Type	Location	Notes
mkdebian_stretch.sh	<design name>/os/petalinux	create Debian image
mkubuntu_BionicBeaver.sh	<design name>/os/petalinux	create Ubuntu image

Additional design sources

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Debian SD-Image	*.img	Debian Image for SD-Card
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Prebuilt files (only on ZIP with prebult content)

Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "HDMI0701" Reference Design

Design Flow

Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

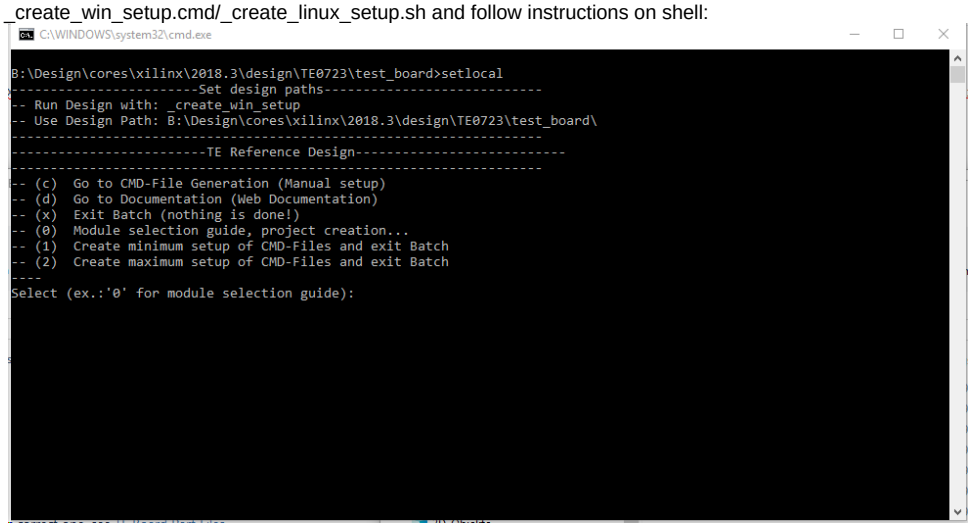
See also:

- AMD Development Tools#XilinxSoftware-BasicUserGuides
- TE Reference Designs Overview
- Project Delivery - AMD devices

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
    a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see also TE Board Part Files
5. Create XSA and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported XSA
    a. XSA is exported to "prebuilt\hardware\<short name>"
    Note: HW Export from Vivado GUI create another path as default workspace.
    Create Linux images on VM, see PetaLinux KICKstart
        i. Use TE Template from /os/petalinux
    c. Build the Debian image/Ubuntu image file with executing the "mkdebian_stretch.sh"/"mkubuntu_BionicBeaver.sh" file in Linux Terminal
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
    a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with Vitis
    a. Run on Vivado TCL: TE::sw_run_vitis -all
    Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
    Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: AMD Development Tools#XilinxSoftwareProgrammingandDebugging

Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
    a. Select assembly version
    b. Validate selection
    c. Select Create and open delivery binary folder
       Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

QSPI

Not used in this Example.

SD

1. Format the SD Card with SD Card Formatter or other tool
2. Write the Debian image or Ubuntu image file on SD Card with Win32DiskImager
3. Copy Petalinux image.ub and Boot.bin on SD-Card.
    - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries
    - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
4. Set Boot Mode to SD-Boot.
    - Depends on Carrier, see carrier TRM.
5. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section TE0820 HDMI701#Programming
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode
   Note: On TE0701 Default Firmware Boot Mode is selected via SD card (insered SD Card for SD Boot Mode)
4. Connect HDMI to Monitor
5. Connect USB Adapter with Hub and Mouse+Keyboard
6. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

Linux

1. Open Serial Console (e.g. putty)
    a. Speed: 115200
    b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
    a. User Name: root
    b. Password: root
3. You can use Linux shell now.
4. Debian Desktop
    a. Debian Desktop will be started automatically
    b. Use connected mouse + keyboard for interaction with GUI
    c. Web Browser Dillo open console and type dillo or use browser
    d. open console and start video or audio with "mplayer <video or audio file>"
5. Ubuntu Desktop
    a. Ubuntu Desktop will be started automatically
    b. Use connected mouse + keyboard for interaction with GUI
    c. Web Browser Mozilla firefox can be used.
    d. Audio or Vider file can also be performed directly in GU

Vivado HW Manager

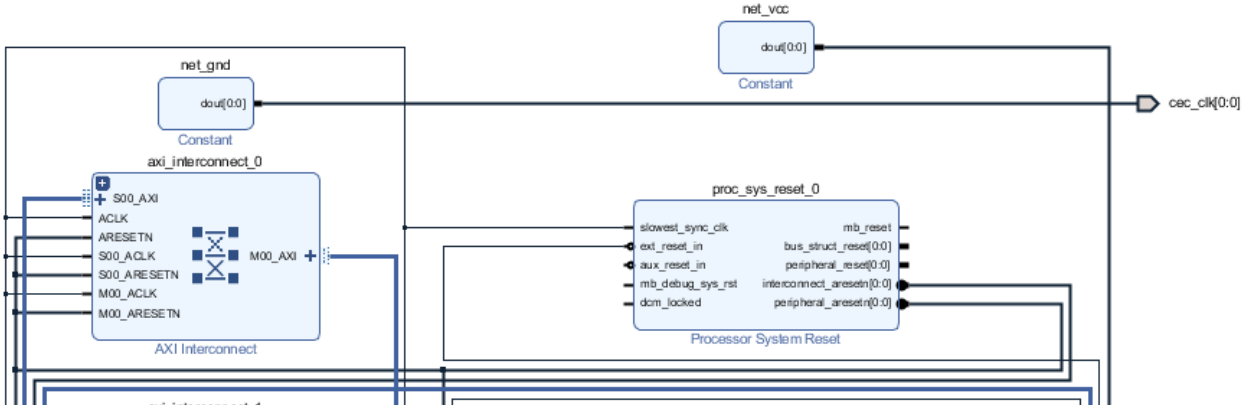
Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

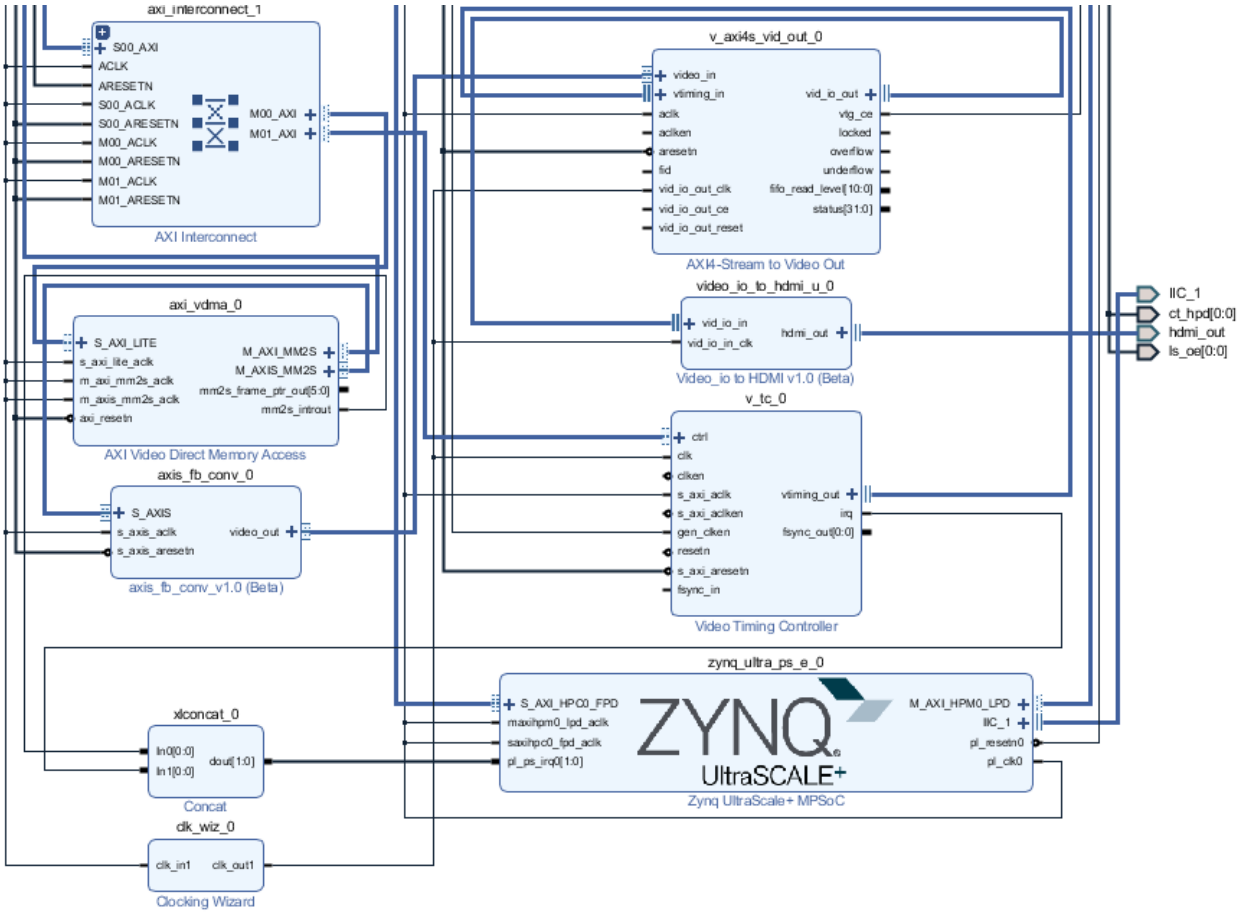
- Control:
- Monitoring:

Vivado Hardware Manager

System Design - Vivado

Block Design


net_vcc
dout[0:0]
Constant
net_gnd
dout[0:0]
Constant
cec_clk[0:0]
axi_interconnect_0
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset



Block Design

PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
I2C1	EMIO
UART0	MIO
GPIO0	MIO
SWDT0..1	

TTC0..3	
GEM3	MIO
USB0	MIO

PS Interfaces

Constrains

Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

_i_hdmi.xdc

```
 TODO replace loc constrains with correct one for TE0820
#
# TE0701 I2C Bus
#
set_property PACKAGE_PIN P7 [get_ports IIC_1_scl_io]
set_property PACKAGE_PIN P6 [get_ports IIC_1_sda_io]
set_property IOSTANDARD LVCMOS18 [get_ports IIC_1_scl_io]
set_property IOSTANDARD LVCMOS18 [get_ports IIC_1_sda_io]

#
# ADV7511 Interface
#
set_property PACKAGE_PIN L6 [get_ports hdmi_out_clk]
set_property PACKAGE_PIN L7 [get_ports hdmi_out_de]
set_property PACKAGE_PIN K4 [get_ports hdmi_out_hsync]
set_property PACKAGE_PIN K3 [get_ports hdmi_out_vsync]
set_property PACKAGE_PIN T6 [get_ports {hdmi_out_data[0]}]
set_property PACKAGE_PIN R6 [get_ports {hdmi_out_data[1]}]
set_property PACKAGE_PIN V9 [get_ports {hdmi_out_data[2]}]
set_property PACKAGE_PIN U9 [get_ports {hdmi_out_data[3]}]
set_property PACKAGE_PIN T7 [get_ports {hdmi_out_data[4]}]
set_property PACKAGE_PIN N8 [get_ports {hdmi_out_data[5]}]
set_property PACKAGE_PIN R7 [get_ports {hdmi_out_data[6]}]
set_property PACKAGE_PIN N9 [get_ports {hdmi_out_data[7]}]
set_property PACKAGE_PIN Y8 [get_ports {hdmi_out_data[8]}]
set_property PACKAGE_PIN V8 [get_ports {hdmi_out_data[9]}]
set_property PACKAGE_PIN W8 [get_ports {hdmi_out_data[10]}]
set_property PACKAGE_PIN U8 [get_ports {hdmi_out_data[11]}]
set_property IOSTANDARD LVCMOS18 [get_ports hdmi_*]

set_property PACKAGE_PIN H7 [get_ports {cec_clk[0]}]
set_property PACKAGE_PIN M8 [get_ports {ct_hpd[0]}]
set_property PACKAGE_PIN J7 [get_ports {ls_oe[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {cec_clk[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {ct_hpd[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {ls_oe[0]}]
```

Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis

Application

Template location: ./sw_lib/sw_apps/

zynqmp_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration
    - ETH+OTG Reset over MIO
    - DMA for HDMI

zynqmp_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

zynqmp_pmufw

Xilinx default PMU firmware.

U-Boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Select Image Packaging Configuration ==> Root filesystem type ==> Select SD Card

Changes:

- CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- CONFIG_SUBSYSTEM_ETHERNET_PSU_ETHERNET_3_MAC=""
- # CONFIG_SUBSYSTEM_ROOTFS_INITRAMFS is not set
- # CONFIG_SUBSYSTEM_ROOTFS_INITRD is not set
- # CONFIG_SUBSYSTEM_ROOTFS_JFFS2 is not set
- # CONFIG_SUBSYSTEM_ROOTFS_NFS is not set
- CONFIG_SUBSYSTEM_ROOTFS_SD=y
- # CONFIG_SUBSYSTEM_ROOTFS_OTHER is not set
- # CONFIG_SUBSYSTEM_BOOTARGS_AUTO is not set
- CONFIG_SUBSYSTEM_USER_CMDLINE="console=ttyPS0,115200 earlycon clk_ignore_unused earlyprintk root=/dev/mmcblk1p2 rootfstype=ext4 rw rootwait cma=256M"
- CONFIG_SUBSYSTEM_DEVICETREE_FLAGS=""
- # CONFIG_SUBSYSTEM_DTB_OVERLAY is not set
- # CONFIG_SUBSYSTEM_REMOVE_PL_DTB is not set

U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- CONFIG_I2C_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50
- CONFIG_SYS_I2C_EEPROM_BUS=0
- CONFIG_SYS_EEPROM_SIZE=256
- CONFIG_SYS_EEPROM_PAGE_WRITE_BITS=0
- CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS=0
- CONFIG_SYS_I2C_EEPROM_ADDR_LEN=1
- CONFIG_SYS_I2C_EEPROM_ADDR_OVERFLOW=0

Device Tree

```
/include/ "system-conf.dtsi"
/ {
        chosen {
                    xlnx,eeprom = &eeprom;
                    bootargs= "console=ttyPS0,115200 earlycon clk_ignore_unused earlyprintk root=/dev/mmcblk1p2
rootfstype=ext4 rw rootwait cma=256M";

          };
};


/ {
        #address-cells = <2>;
        #size-cells = <2>;
        memory@0{
          device-type = "memory";
          reg = <0x000000000 0x00000000 0x00000000 0x80000000>;
        };
        reserved-memory {
                #address-cells = <2>;
                #size-cells = <2>;
                ranges;
                hdmi_fb_reserved_region: framebuffer@7FC00000 {
                    compatible = "removed-dma-pool";
                    //compatible = "shared-dma-pool";
                    //compatible = "xlnx,reserved-memory";
                    no-map;
                    reg = <0x0 0x7FC00000 0x0 0x400000>;
                };
             };

        hdmi_fb: framebuffer@0x7FC00000 {           // HDMI out
                compatible = "simple-framebuffer";
                reg = <0x0 0x7FC00000 0x0 (1280 * 720 * 4)>;    // 720p
                width = <1280>;                         // 720p
                height = <720>;                         // 720p
                stride = <(1280 * 4)>;                  // 720p
                format = "a8b8g8r8";
```

```
                status = "okay";
        };
};

&axi_vdma_0 {
   status = "disabled";
};

&v_tc_0 {
    //xilinx-vtc: probe of 43c20000.v_tc failed with error -2
    status = "disabled";
};

/* SDIO */

&sdhci1 {
   status = "okay";
   disable-wp;
   no-1-8-v;
};

/* ETH PHY */
&gem3 {

        status = "okay";
  ethernet_phy0: ethernet-phy@0 {
                compatible = "marvell,88e1510";
                device_type = "ethernet-phy";
                    reg = <1>;
        };
};
/* USB 2.0 */

/* USB  */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
          snps,dis_u2_susphy_quirk;
          snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};




/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
```

```
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

&i2c0 {
  eeprom: eeprom@50 {
     compatible = "atmel,24c08";
     reg = <0x50>;
  };
};
```

Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_CPU_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG_EDAC_CORTEX_ARM64=y
- CONFIG_FB_SIMPLE
- CONFIG_LOGO
- CONFIG_LOGO_LINUX_MONO
- CONFIG_LOGO_LINUX_VGA16
- CONFIG_LOGO_LINUX_CLUT224

Rootfs

File System will be generated with Debian script or Ubuntu script (mkdebian_stretch.sh/mkubuntu_BionicBeaver.sh)

Applications

Applications will be generated with Debian script or Ubuntu script (mkdebian_stretch.sh/mkubuntu_BionicBeaver.sh)

Additional Software

SI5338

File location <design name>/misc/Si5338/Si5338-*.slabtimeproj

General documentation how you work with these project will be available on Si5338

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
Error rendering macro 'page-info' Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	**Error rendering macro 'page-info'** Ambiguous method overloading for method jdk.proxy279.$Proxy4022#hasContentLevelPermission. Cannot resolve which method to invoke for [null, class java.lang.String, class com.atlassian.confluence.pages.Page] due to overlapping prototypes between: [interface com.atlassian.confluence.user.ConfluenceUser, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject] [interface com.atlassian.user.User, class java.lang.String, class com.atlassian.confluence.core.ContentEntityObject]	• fix brocken links
2020-03-30	v.5	Mohsen Chamanbaz	• 2019.2 release

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Document change history.

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REACH, RoHS and WEEE

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Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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